General Purpose I/O GPIO (pin E10)

The GPI pin is a single assignable general-purpose digital input or output that is available only to the management SoC and cannot be assigned to the user project area. On the test board provided with the completed user projects, this pin is used to enable the voltage regulators generating the user area power supplies.

The basic function of the GPIO is illustrated below. All writes to **`reg_gpio_data`** are registered. All reads from **reg_gpio_data** are immediate.

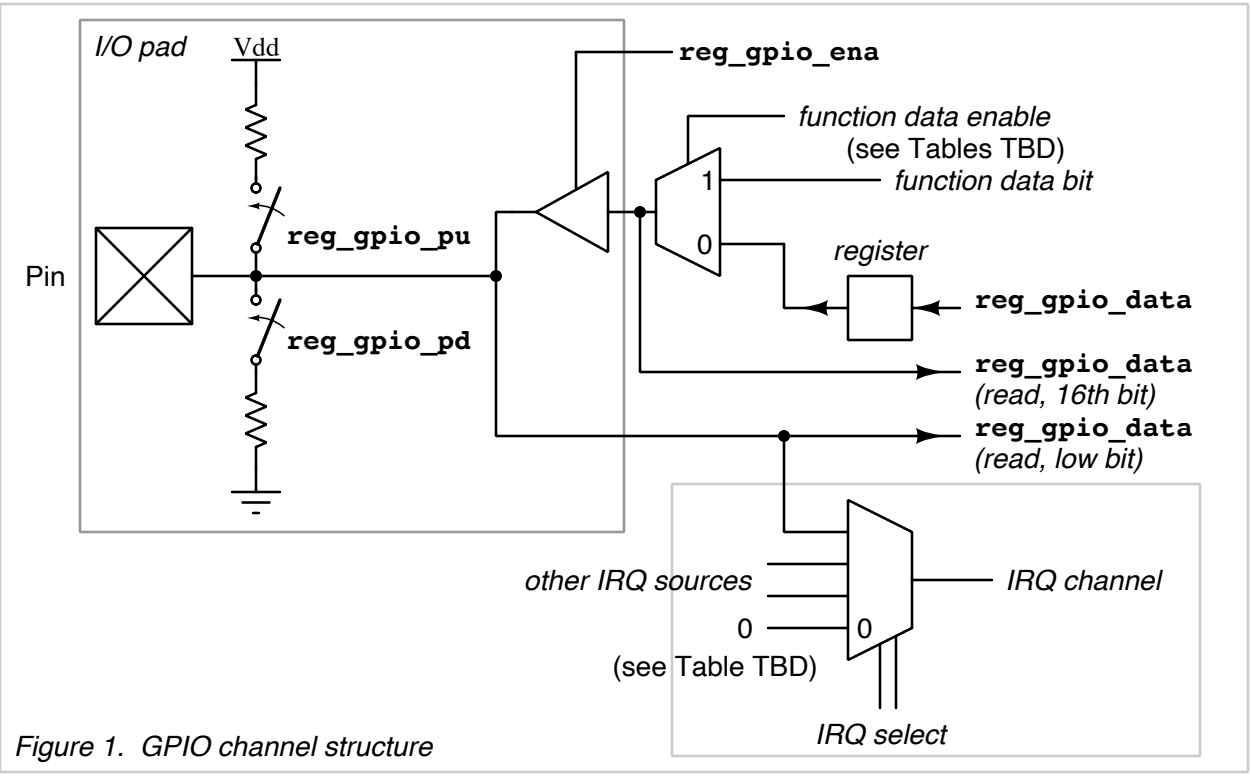

Figure 1. GPIO channel structure

GPIO memory address map:

C header name	*address*	*description*
`reg_gpio_data`	**`0x21000000`**	GPIO input/output (low bit) GPIO output readback (16th bit)
`reg_gpio_ena`	**`0x21000004`**	GPIO output enable (0 = output, 1 = input)
`reg_gpio_pu`	**`0x21000008`**	GPIO pullup enable (1 = pullup, 0 = none)
`reg_gpio_pd`	**`0x2100000c`**	GPIO pulldown enable (1 = pulldown, 0 = none)
`reg_pll_out_dest`	**`0x2f000000`**	PLL clock output destination (low bit)
`reg_trap_out_dest`	**`0x2f000004`**	Trap output destination (low bit)
`reg_irq7_source`	**`0x2f000008`**	IRQ 7 input source (low bit)

GPIO description, continued.

In the memory-mapped register descriptions below, each register is shown as 32 bits corresponding to the data bus width of the wishbone bus. Addresses, however, are in bytes. Depending on the instruction and data type, the entire 32-bit register can be read in one instruction, or one 16-bit word, or one 8-bit byte.

Table 1 **reg_gpio_data**

0x21000003								**0x21000002**								**0x21000001**								**0x21000000**								address
GPIO output readback																GPIO input/output																value
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

Writing to the address low bit always sets the registered value at the GPIO.
Writing to address bit 16 has no effect.
Reading from the address low bit reads the value at the chip pin.
Reading from address bit 16 reads the value at the multiplexer output (see diagram).

Table 2 **reg_gpio_ena**

0x21000007								**0x21000006**								**0x21000005**								**0x21000004**								address
(undefined, reads zero)																GPIO output enable																value
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

Bit 0 corresponds to the GPIO channel enable.
Bit value 1 indicates an output channel; 0 indicates an input.

Table 3 **reg_gpio_pu**

0x2100000b								**0x2100000a**								**0x21000009**								**0x21000008**								address
(undefined, reads zero)																GPIO pin pull-up																value
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

Bit 0 corresponds to the GPIO channel pull-up state.
Bit value 1 indicates pullup is active; 0 indicates pullup inactive.

Table 4 **reg_gpio_pd**

0x2100000f								**0x2100000e**								**0x2100000d**								**0x2100000c**								address
(undefined, reads zero)																GPIO pin pull-down (inverted)																value
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

Bit 0 corresponds to the GPIO channel pull-down state.
Bit value 1 indicates pullup is active; 0 indicates pulldown is inactive.