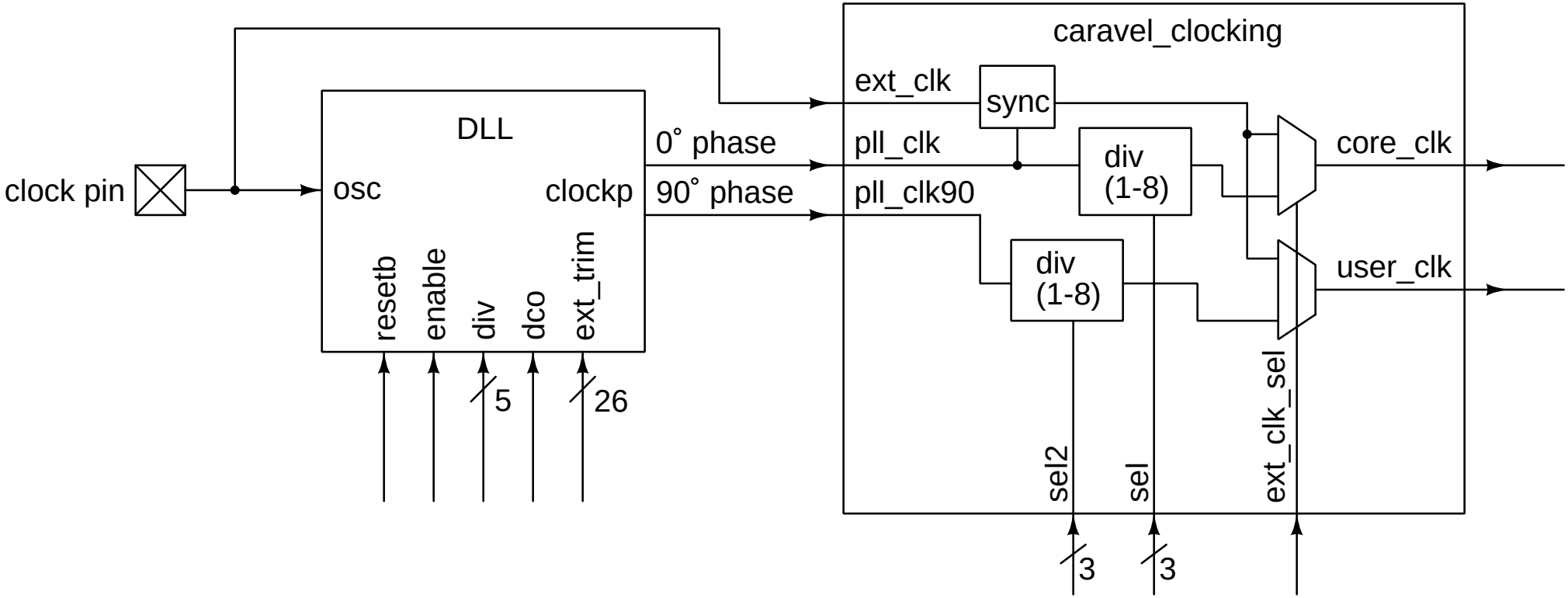
caravel_clocking
ext_clk
sync
pll_clk
div
(1-8)
core_clk
pll_clk90
div
(1-8)
user_clk
DLL
0° phase
90° phase
clock pin
osc
clockp
resetb
enable
div
dco
ext_trim
5
26
sel2
sel
ext_clk_sel
3
3