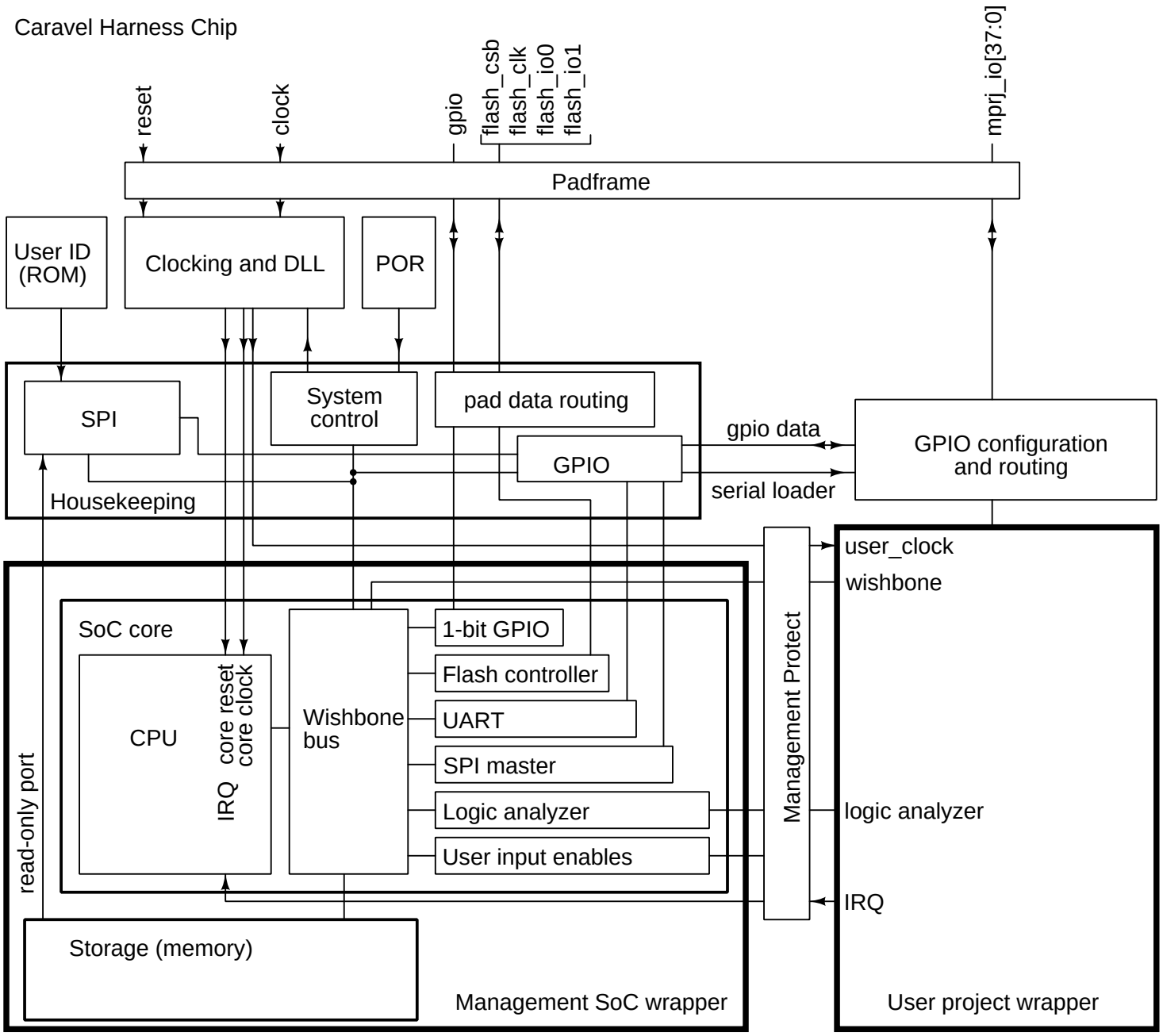
Caravel Harness Chip
reset
clock
gpio
flash_csb
flash_clk
flash_io0
flash_io1
mprj_io[37:0]
Padframe
User ID (ROM)
Clocking and DLL
POR
SPI
System control
pad data routing
GPIO
Housekeeping
gpio data
serial loader
GPIO configuration and routing
user_clock
wishbone
logic analyzer
IRQ
Management Protect
SoC core
CPU
IRQ
core reset
core clock
Wishbone bus
1-bit GPIO
Flash controller
UART
SPI master
Logic analyzer
User input enables
read-only port
Storage (memory)
Management SoC wrapper
User project wrapper