SPI Master spi sdi (pin E9), spi csb (pin E8), spi sck (pin F8), and spi sdo (pin F9)

Table 14 **reg_spi_config**

0x24000003								0x24000002								0x24000001								0x24000000								address
(undefined, reads zero)																SPI master configuration																value
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

Configuration bit defintions

Bit 15	Housekeeping	0 = SPI master connected to external pins 1 = SPI master connected directly to housekeeping SPI
Bit 14	SPI interrupt enable	0 = interrupt disabled 1 = interrupt enabled
Bit 13	SPI system enable	0 = SPI disabled 1 = SPI enabled
Bit 12	stream	0 = apply/release CSB separately for each byte 1 = apply CSB until stream bit is cleared (manually)
Bit 11	mode	0 = read and change data on opposite SCK edges 1 = read and change data on the same SCK edge
Bit 10	invert SCK	0 = normal SCK 1= inverted SCK
Bit 9	invert CSB	0 = normal CSB (low is active) 1 = inverted CSB (high is active)
Bit 8	MLB	0 = msb first 1 = lsb first
Bits 7–0	prescaler	count (in master clock cycles) of 1/2 SCK cycle (default value 2)

All configuration bits other than the prescaler default to value zero.

Table 15 **reg_spi_data**

0x24000007								0x24000006								0x24000005								0x24000004								address
(undefined, reads zero)																								SPI data								value
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

The byte at 0x24000004 holds the SPI data (either read or write)

Reading to and writing from the SPI master is simply a matter of setting the required values in the configuration register, and writing values to or reading from reg_spi_data. The protocol is similar to the UART. A write operation will stall the CPU if an incomplete SPI transmission is still in progress. Reading from the SPI will also stall the CPU if an incomplete SPI transmission is still in progress. There is no FIFO buffer for data. Therefore SPI reads and writes are relatively expensive operations that tie up the CPU, but will not lose or overwrite data. Note that there is no FIFO associated with the SPI master.