Counter-Timer 0

The counter/timer is a general-purpose 32-bit adder and subtractor that can be configured for a variety of timing functions including one-shot counts, continuous timing, and interval interrupts. At a core clock rate of 80 MHz, the longest single time interval is 26.84 seconds.

Table 16 **reg_timer0_config**

0x22000003	0x22000002	0x22000001	0x22000000	address
(undefined, reads zero)			Timer config	value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

Timer configuration bit definitions

Bit 3	Counter/timer enable	1 = counter/timer enabled 0 = counter/timer disabled
Bit 2	Oneshot mode	1 = oneshot mode 0 = continuous mode
Bit 1	Updown	1 = count up 0 = count down
Bit 0	Interrupt enable	1 = interrupt enabled 0 = interrupt disabled

Table 17 **reg_timer0_value**

0x22000007	0x22000006	0x22000005	0x22000004	address
Timer value				value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

The value in this register is the current value of the counter. Value is 32 bits. The register is read-write and can be used to reset the timer.

Table 18 **reg_timer0_data**

0x2200000b	0x2200000a	0x22000009	0x22000008	address
Timer data				value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

The value in this register is the reset value for the comparator.

When enabled, the counter counts up or down from the value set in reg_timer_value at the time the counter is enabled. If counting up, the count continues until the counter reaches reg_timer_data. If counting down, the count continues until the counter reaches zero.

In continuous mode, the counter resets to zero if counting up, and resets to the value in reg_timer_data if counting down, and the count continues immediately. If the interrupt is enabled, the counter will generate an interrupt on every cycle.

In one-shot mode, the counter triggers an interrupt (IRQ channel 10; see next page) when it reaches the value of reg_timer_data (up count) or zero (down count), and stops.

Note: When the counter/timer is disabled, the reg_timer_value remains unchanged, which puts the timer in a hold state. When re-enabled, counting resumes. To reset the timer, write zero to the reg_timer_value register.

Counter-Timer 1

The second counter/timer is functionally identical to the first, with different memory mapped addresses for the controls, as shown in the tables below.

Table 19 **reg_timer1_config**

0x23000003	0x23000002	0x23000001	0x23000000	address
(undefined, reads zero)			Timer config	value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

Timer configuration bit definitions

Bit 3	Counter/timer enable	1 = counter/timer enabled 0 = counter/timer disabled
Bit 2	Oneshot mode	1 = oneshot mode 0 = continuous mode
Bit 1	Updown	1 = count up 0 = count down
Bit 0	Interrupt enable	1 = interrupt enabled 0 = interrupt disabled

Table 20 **reg_timer1_value**

0x23000007	0x23000006	0x23000005	0x23000004	address
Timer value				value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

The value in this register is the current value of the counter. Value is 32 bits. The register is read-write and can be used to reset the timer.

Table 21 **reg_timer1_data**

0x2300000b	0x2300000a	0x23000009	0x23000008	address
Timer data				value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

The value in this register is the reset value for the comparator.

When enabled, the counter counts up or down from the value set in reg_timer_value at the time the counter is enabled. If counting up, the count continues until the counter reaches reg_timer_data. If counting down, the count continues until the counter reaches zero.

In continuous mode, the counter resets to zero if counting up, and resets to the value in reg_timer_data if counting down, and the count continues immediately. If the interrupt is enabled, the counter will generate an interrupt on every cycle.

In one-shot mode, the counter triggers an interrupt (IRQ channel 11; see next page) when it reaches the value of reg_timer_data (up count) or zero (down count), and stops.

Note: When the counter/timer is disabled, the reg_timer_value remains unchanged, which puts the timer in a hold state. When re-enabled, counting resumes. To reset the timer, write zero to the reg_timer_value register.