GPIO description, continued.

Table 5 **reg_pll_out_dest**

0x2f000003	0x2f000002	0x2f000001	**0x2f000000**	address
(undefined, reads zero)			PLL clock dest.	value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

The low bit of this register directs the output of the core clock to the GPIO channel, according to the following table:

Register byte **0x2f000000** value		Clock output directed to this channel
0	**0**	(none)
1	**1**	Core PLL clock to GPIO out

Note that a high rate core clock (*e.g.,* 80 MHz) may be unable to generate a full swing on the GPIO output.

Table 6 **reg_trap_out_dest**

0x2f000007	0x2f000006	0x2f000005	**0x2f000004**	address
(undefined, reads zero)			trap signal dest.	value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

The low bit of this register directs the output of the processor trap signal to the GPIO channel, according to the following table:

Register byte **0x2f000004** value		Trap signal output directed to this channel
0	**0**	(none)
1	**1**	GPIO

Table 7 **reg_irq7_source**

0x2f00000b	0x2f00000a	0x2f000009	**0x2f000008**	address
(undefined, reads zero)			IRQ 7 source	value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

The low bit of this register directs the input of the GPIO to the processor's IRQ7 channel, according to the following table:

Register byte **0x2f000008** value		This channel directed to IRQ channel 7
0	**00**	(none)
1	**01**	GPIO