Interrupts (IRQ)

The interrupt vector is set to memory addres 0 (bottom of SRAM). The program counter switches to this location when an interrupt is received. To enable interrupts, it is necessary to copy an interrupt handler to memory location 0. The PicoRV32 defines 32 IRQ channels, of which the Caravel chip uses only a handful, as described in the table below. All IRQ channels not in the list below always have value zero.

Table 19 CPU IRQ channel definitions

IRQ channel	*description*
4	UART data available
5	IRQ external pin (pin E5)
6	Housekeeping SPI IRQ
7	Assignable interrupt (see Table 7)
9	SPI master data available, when enabled (see Table 14)
10	Timer 0 expired, when enabled (see Table 16)
11	Timer 1 expired, when enabled (see Table 19)

The Caravel PicoRV32 implementation does not enable IRQ QREGS (see PicoRV32 description).

The handling of interrupts is beyond the scope of this document (see RISC-V instruction set description). All interrupts are masked and must be enabled in software.

Management area SRAM

The Caravel chip has an on-board memory of 256 words of width 32 bits. The memory is located at address 0 (zero). There are additional blocks of memory above this area, size and location TBD.

Storage area SRAM

The Caravel chip has a “storage area” SRAM block that is auxiliary space that can be used by either the management SoC or the user project, through the wishbone bus interface. The storage area is connected into the user area 2 power supply, and so is nominally considered to be part of the user area.

The storage area may be used as an experimentation area for OpenRAM, so for any user project making use of this space, the user should notify efabless of their requirement for the size and configuration of the SRAM block.