QSPI Flash interface flash io0–1 (pins D10 to D9), flash csb (pin C10), and flash clk (pin D8)

The QSPI flash controller is automatically enabled on power-up, and will immediately initiate a read sequence in single-bit mode with pin "flash io0" acting as SDI (data from flash to CPU) and pin "flash io1" acting as SDO (data from CPU to flash). Protocol is according to, *e.g.,* Cypress S25FL256L.

The initial SPI instruction sequence is as follows:

0xFF	Mode bit reset
0xAB	Release from deep power-down
0x03	Read w/3 byte address
0x00	Program start address (**0x10000000**) (3 bytes) (upper byte is ignored)
0x00	
0x00	

The QSPI flash continues to read bytes, either sequentially on the same command, or issuing a new read command to read from a new address.

The behavior of the QSPI flash controller can be modified by changing values in the register below:

Table 10 **reg_spictrl**

0x2d000003								**0x2d000002**								**0x2d000001**								**0x2d000000**								address
(unused)								(see below)								(unused)								(see below)								value
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bit

mask bit	default	description
31	1	QSPI flash interface enable
22–20	0	Access mode (see table below)
19–16	8	Dummy clock cycle count
11–8	0	Bit-bang OE FLASH_IO3–FLASH_IO0
5	0	Bit-bang FLASH_CSB
4	0	Bit-bang FLASH_CLK
3–0	0	Bit-bang value FLASH_IO3–FLASH_IO0

Access mode bit selection (bits 22–20):

0	**000**	Single bit per clock
1	**001**	Single bit per clock (same as 0)

All additional modes (QSPI dual and quad modes) cannot be used, as the management SoC only has pins for data lines 0 and 1.

The SPI flash can be accessed by bit banging when the enable is off. To do this from the CPU, the entire routine to access the SPI flash must be read into SRAM and executed from the SRAM.

Interrupt IRQ (pin E5)

The interrupt pin triggers the CPU interrupt channel 5.