Caravel SoC

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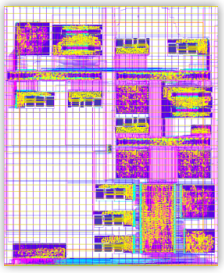
Description

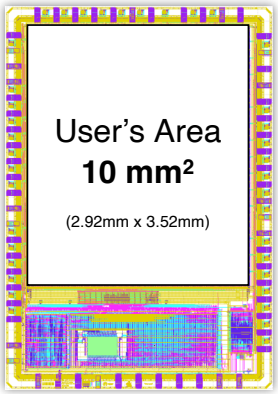
Caravel is a design template for creating your own semi-custom ASIC as part of Efabless chipIgnite solution with the open-source SKY130 PDK for the 130nm CMOS Skywater technology process . Caravel includes a 10 mm^2 user area on the chip for implementing your custom design.

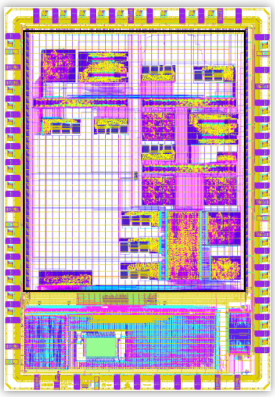
The carrier chip provides all the infrastructure required for building a chip including IO and power, clock, reset, and a management SoC that can be used to drive your project. The management SoC includes a RISC-V processor, memory and a wishbone bus that extends into the user area for connecting your own peripherals.

Features

- 38 programmable IO
- 10 mm^2 of user project area
- VexRiscv core with serial and SPI debug ports
- 1.5 kbytes of RAM
- SPI Flash controller supporting XIP
- UART, SPI and GPIO ports
- 128 port logic analyzer
- Counter / timer
- 32-bit wishbone bus extending to the user project area
- 6 user interrupts
- DLL, PoR
- 33 MHz
- User power domains:
  - 2 digital domains, 1.71 to 1.89 V
  - 2 analog domain, 3.0 to 5.5 V
- Other power domains:
  - vccd, SoC core voltage, 1.8V nom
  - vddio / vdda, IO output driver voltage, 3.3 to 5.0V nom
- Packages available
  - QFN 64L
  - WCSP 60 ball
  - Bare die
- Temperature range, 0 to 70 deg C







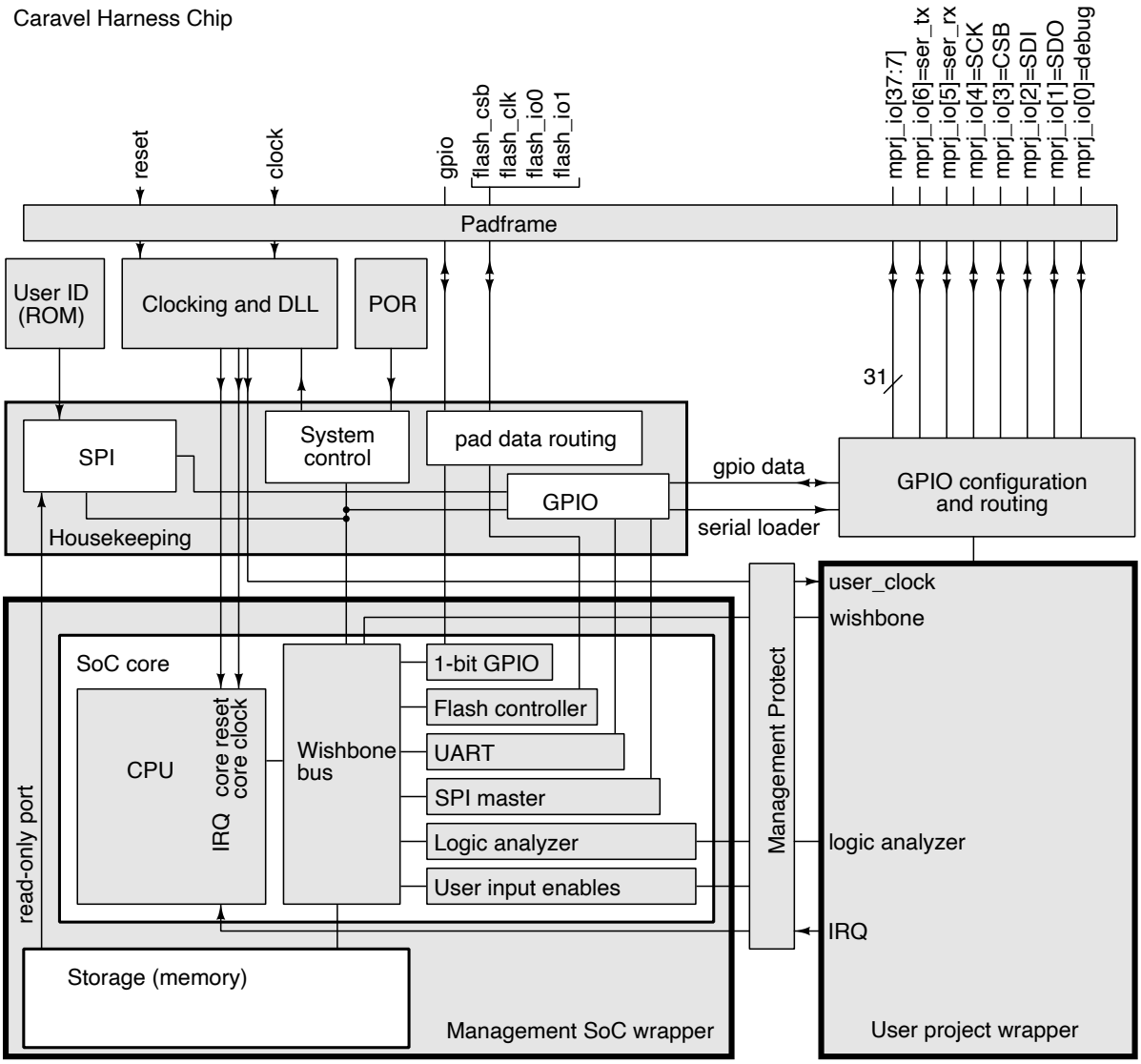
License

Caravel is an open-source design licensed under the terms of Apache 2.0. The design can be found at GitHub in the efabless/caravel repository.

Contents

1. Functional Overview

1.1. Functional Block Diagram



1.2. Your design

Caravel provides an SoC design template for implementing a custom digital, analog or mixed signal design within a 10mm2 user project area in the center of the chip. The user project area is integrated with Caravel through a user_project_

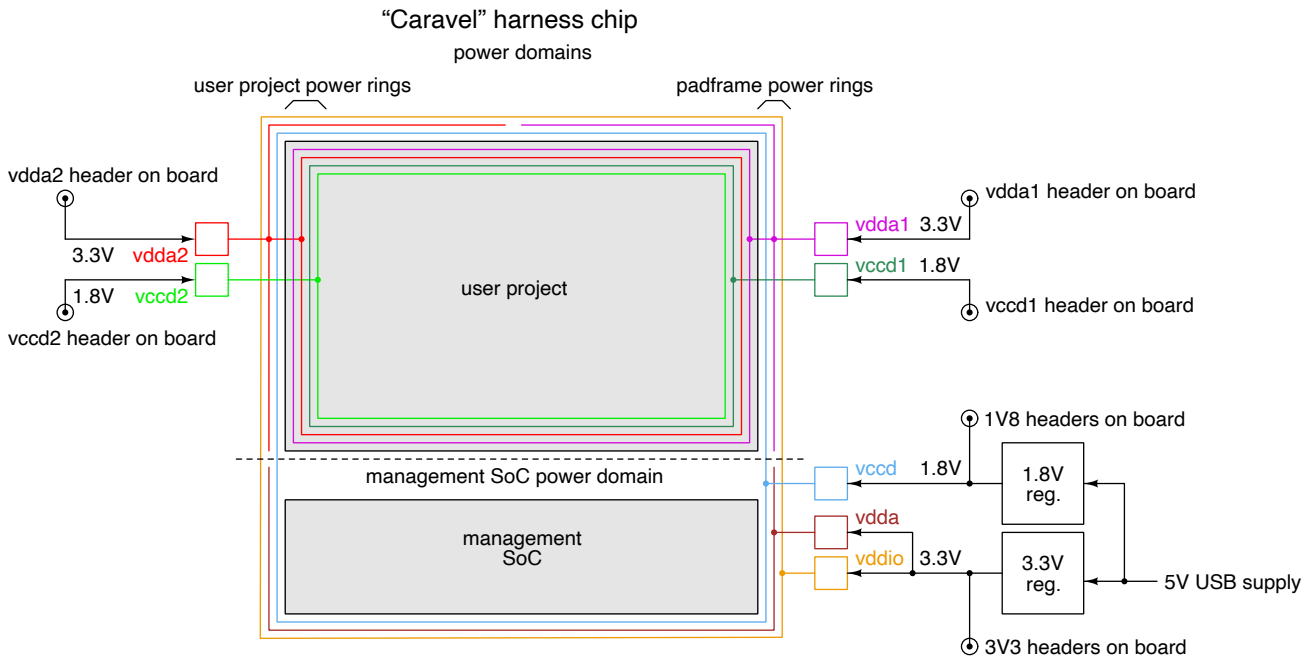
wrapper block.

1.3. Caravel

Caravel provides the infrastructure for the complete chip. This includes a padframe with power, IO and ESD protection circuitry. It also includes a VexRiscv microcontroller based on RISC-V with memory and peripherals.

1.4. Power supply domains and power grid

The caravel chip provides four voltage domains to the user project area, 2 analog (3.3V - vdda1, vdda2) and 2 digital (1.8V - vccd1, vccd2). Supplies for padframe and gpio outputs are provided by vddio and vdda. Within the GPIO cells, vswitch is connected to vddio and vcchib is connected to vccd. Core voltage domain for the management area is provided by vccd (1.8V).



1.5. GPIO pads

Caravel provides 38 programmable GPIO pads. The GPIO pads are multi-purpose

capable of being configured for numerous applications, including digital input, output, analog signaling, with slew rate control, transition level control, and weak pull-up and pull-down functions.

The GPIO pads are configured to operate either under the control of the management SoC or under the control of the user project. When used under management SoC control, certain pins have certain special functions.

The GPIO pads are configured at design time to provide a desired on power-up state for based on the intended application. The pads can be reconfigured after power-on using firmware or through the housekeeping SPI interface.

1.6. Housekeeping

The housekeeping function provides access to certain system values and controls independently of the CPU. The housekeeping SPI can be accessed even when the CPU is in full reset. Some control registers in the housekeeping SPI affect the behaviour of the CPU in a way that can be potentially detrimental to the CPU operation, such as adjusting the trim value of the digital frequency-locked loop generating the CPU core clock.

Under normal working conditions, the SPI should not need to be accessed unless it is to adjust the clock speed of the CPU. All other functions are purely for test and debug.

The housekeeping SPI can be accessed by the CPU from a running program by enabling the SPI controller, and enabling the bit that connects the internal SPI controller directly to the housekeeping SPI. This configuration then allows a program to read, for example, the user project ID of the chip. See the SPI controller description for details.

1.7. Programming process

The houskeeping function provides a pass-thru mode which allows the SPI flash to be programmed from the same SPI communication channel as the housekeeping SPI, without the need for additional wiring to the SPI flash chip.

1.8. Processor

The processor core is based on a VexRiscv minimal+debug configuration. The core has been configured with 64 bytes of instruction cache. The core has not been con-

figured with compress or multiply instructions.

1.9. Memory

The mangement SoC implements on-board memory 384 words with 32 bit width. The memory is synthesized using standard cells.

1.10. Debug

Debug support is enabled in the core and can be accessed through a dedicated UART port configured as a wishbone master. The baud rate for the port is 9600.

1.11. Wishbone bus

The VexRiscv microcontroller extends a wishbone bus to the user project area. The interface can be used for connecting one or more wishbone slave devices or registers. It can also be used to provide clock and reset signals to the design in the user project area.

1.12. Flash controller

The flash controller supports single mode SPI to a compatible W25Q128JV Flash device. The configuration supports execute-in-place and the CPU reset vector is configured for the beginning of the Flash memory region.

1.13. Interrupts

The processor is configured with interrupts for the Uart and Timer devices. It also supports 6 user IRQS extended to the user project.

1.14. Logic analyzer

The logic analyzer function provides a flexible means to monitor signals from the user project wrapper or drive them from the management core.

The logic analyzer supports 128 signals mapped to separated GPIO in, out and oeb ports.

1.15. SPI controller

The management SoC provides a SPI master controller for connecting to external

SPI slave devices.

1.16. UART

The UART provides general serial communication with the management SoC. The baud rate is configured at 9600.

1.17. Clock system

The external clock functions as the source clock for the entire processor. On start-up, the processor runs at the same rate as the external clock. The processor program may access the Housekeeping SPI to set the processor into PLL mode or DCO free-running mode. In PLL mode, the external clock is multiplied by the feedback divider value to obtain the core clock. In DCO mode, the processor is driven by a trimmed free-running ring oscillator.

1.18. Management GPIO

A single GPIO port is provided from the Management SoC as general indicator and diagnostic for programming or as a means to control functionality off chip.

One example user case is to set an enable for an off-chip LDO enabling a controlled power-up sequence for the user project.

1.19. Counter / timer

Provides a generic Timer core. The Timer is implemented as a countdown timer that can be used in various modes:

Polling : returns current countdown value to software
One-Shot: loads itself and stops when value reaches 0
Periodic: (re-)loads itself when value reaches

2. Pin Configuration Functions and Descriptions

2.1. Pinout descriptions

Pin Name	Type	Description
mprj_io[37:0]	digital I/O	General purpose configurable digital I/O with pullup/pulldown, input or output, enable/disable, analog output, high voltage output, slew rate control. Shared between the user project area and the management SoC.
flash_csb	digital out	Flash SPI controller chip select
flash_clk	digital out	Flash SPI controller clock
flash_io0	digital out	Flash SPI controller data output
flash_io1	digital in	Flash SPI controller data input
clock	digital in	External CMOS 3.3V clock source
resetb	digital in	SoC system reset (sense inverted)
SDO	digital out	Housekeeping serial interface data input
SDI	digital in	Housekeeping serial interface chip select
CSB	digital in	Housekeeping serial interface clock
SCK	digital in	Housekeeping serial interface data output
ser_rx	digital in	UART receive channel
ser_tx	digital out	UART transmit channel
irq	digital in	External interrupt
gpio	digital i/o	Management GPIO/user power enable
JTAG	digital in	JTAG Digital I/O JTAG system access
flash2_csb	digital out	Optional user SPI flash controller enable output (sense inverted)
flash2_sck	digital out	Optional user SPI flash controller clock output
flash2_io0	digital out	Optional user SPI flash controller data output
flash2_io1	digital in	Optional user SPI flash controller data input
spi_sdo	digital in	Serial interface master data input
spi_csb	digital in	Serial interface master chip select
spi_sdi	digital in	Serial interface master clock

Pin Name	Type	Description
spi_sdo	digital out	Serial interface master data output
vddio	3.3V power	ESD and padframe power supply
vdda	3.3V power	Management area power supply
vccd	1.8V power	Management area digital power supply
vssio	ground	ESD and padframe ground
vssa	ground	ESD and padframe ground
vssd	ground	Management area ground
vdda1	3.3V power	User area 1 power supply
vccd1	1.8V power	User area 1 digital power supply
vssa1	ground	User area 1 ground
vssd1	ground	User area 1 digital ground
vdda2	3.3V power	User area 2 power supply
vccd2	1.8V power	User area 2 digital power supply
vssa2	ground	User area 2 ground
vssd2	ground	User area 2 digital ground

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Parameter	Description	Unit	Min	Typ	Max	Conditions
vccd, vccd1, vccd2	Digital supply relative to VSS	V	-0.05	--	1.95	
vdda, vdda1, vdda2, vddio	Analog supply relative to VSS	V	-0.05	--	6	vddio must be equal or greater than vdda
gpio (absolute)	GPIO voltage	V	-0.05	--	vddio+0.5	
	Storage temperature range	C	-25	--	100	
	Maximum junction temperature	C	--	--	125	

3.2. Operating conditions

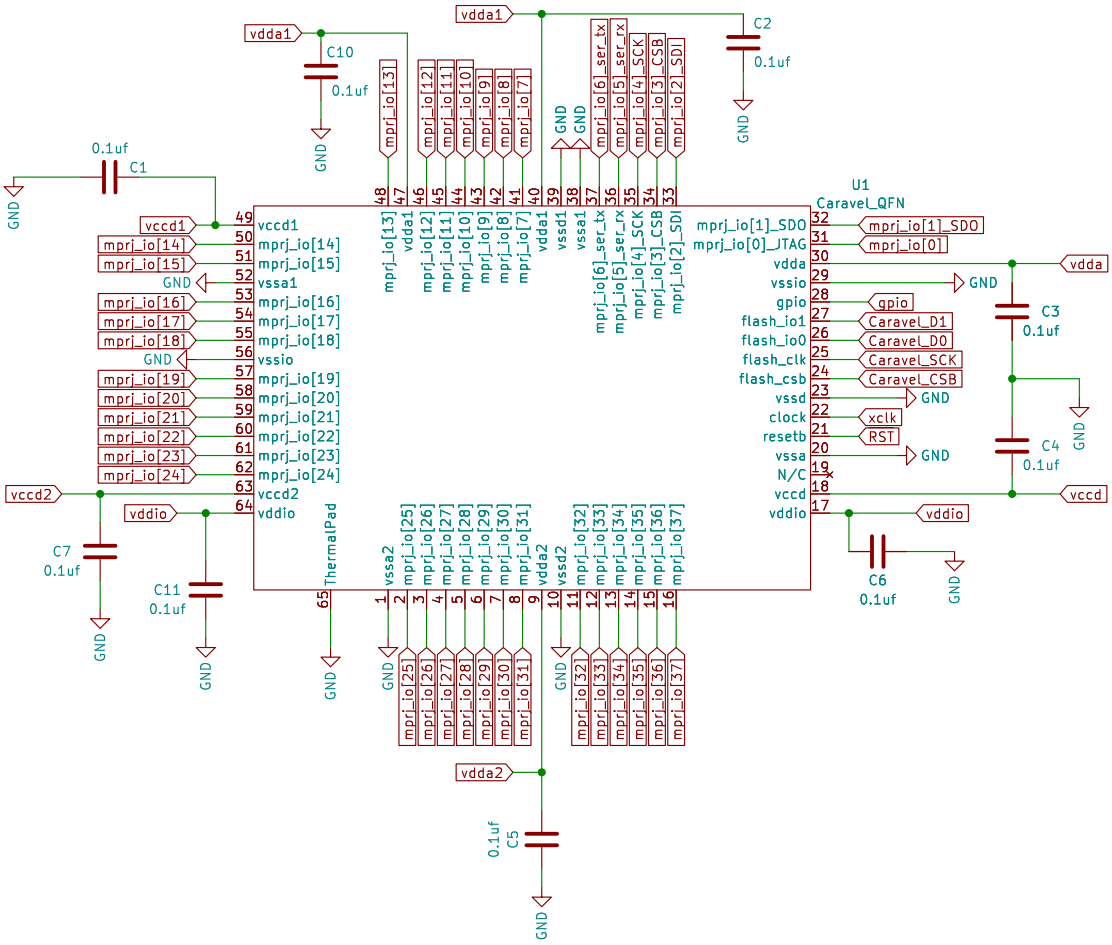
Name	Unit	Min	Nom	Max	Note
Power supplies					
vccd	V	1.62	1.8	1.98	
vccd1	V	1.62	1.8	1.98	
vccd2	V	1.62	1.8	1.98	
vdda	V	1.71	3.3	5.5	
vdda1	V	1.71	3.3	5.5	
vdda2	V	1.71	3.3	5.5	
vddio	V	1.71	3.3	5.5	
IO DC specs					
V_{OH}	V	vddio - 0.6			
V_{OL}	V			0.6	
$V_{IH\ (CMOS)}$	V	0.7 * vddio			
$V_{IL\ (CMOS)}$	V			0.3 * vddio	
$V_{IH\ (TTL)}$	V	02.0			
$V_{IL\ (TTL)}$	V			0.8	
Operating conditions					
Operating temperature range	C	0		70	
Clock and IO frequency	MHz	0		33	
Power on reset release (power up)	V	2.5			
Power on reset assertion (power down)	V			1.0	
Power on rise time delay	msec		50	100	
Reset pulse width	msec	0.1			
Reset input voltage thresholds	V	0.7 * vddio		0.3 * vddio	

4. Applications Information

The following schematic provides an example configuration of a Caravel chip.

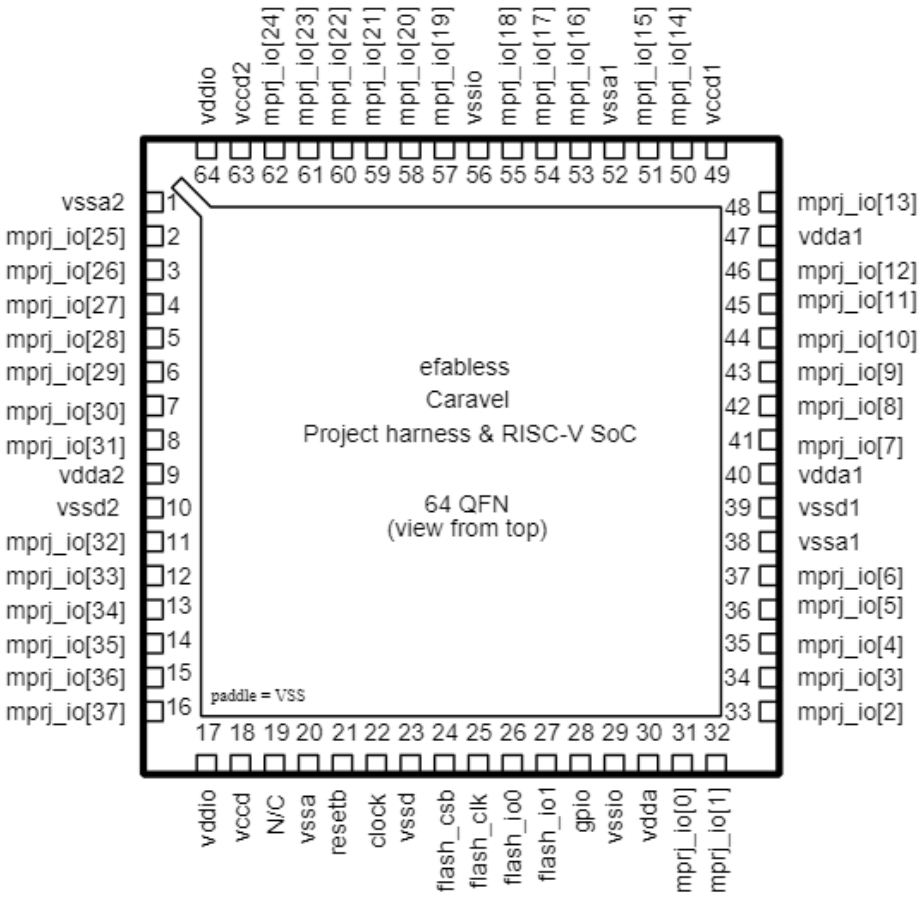
A complete example schematic for an evaluation board supporting the bring up and silicon testing of a Caravel chip can be found at https://github.com/efabless/

caravel_board/tree/main/hardware .



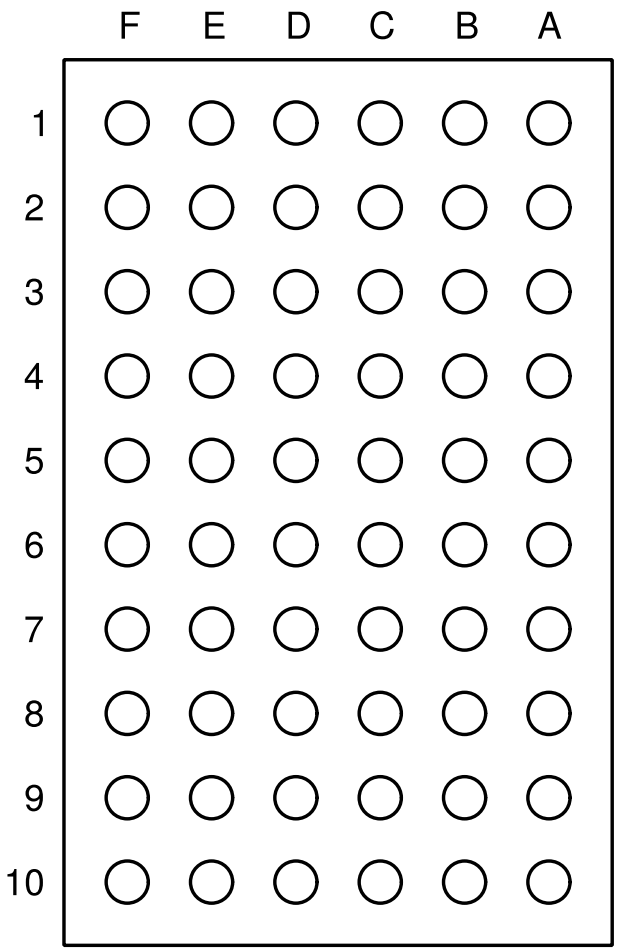
5. Package Information

5.1. 64L QFN package



Package size = 9 mm × 9 mm
Paddle size = 7.63 mm
Pin pitch = 0.5 mm

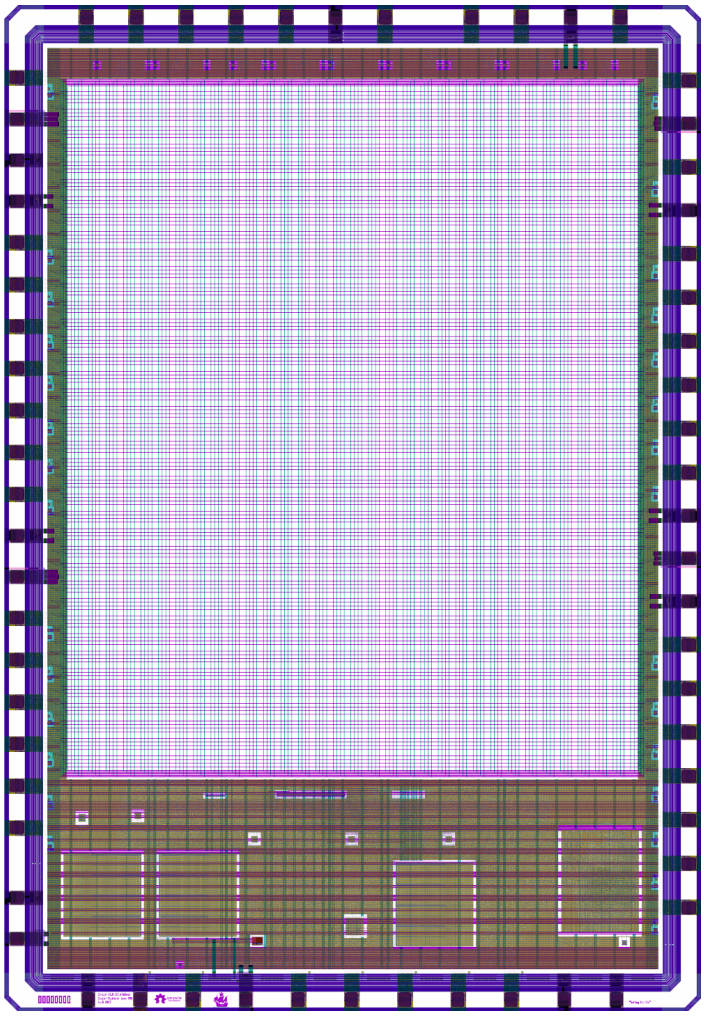
5.2. 60 ball WCSP package



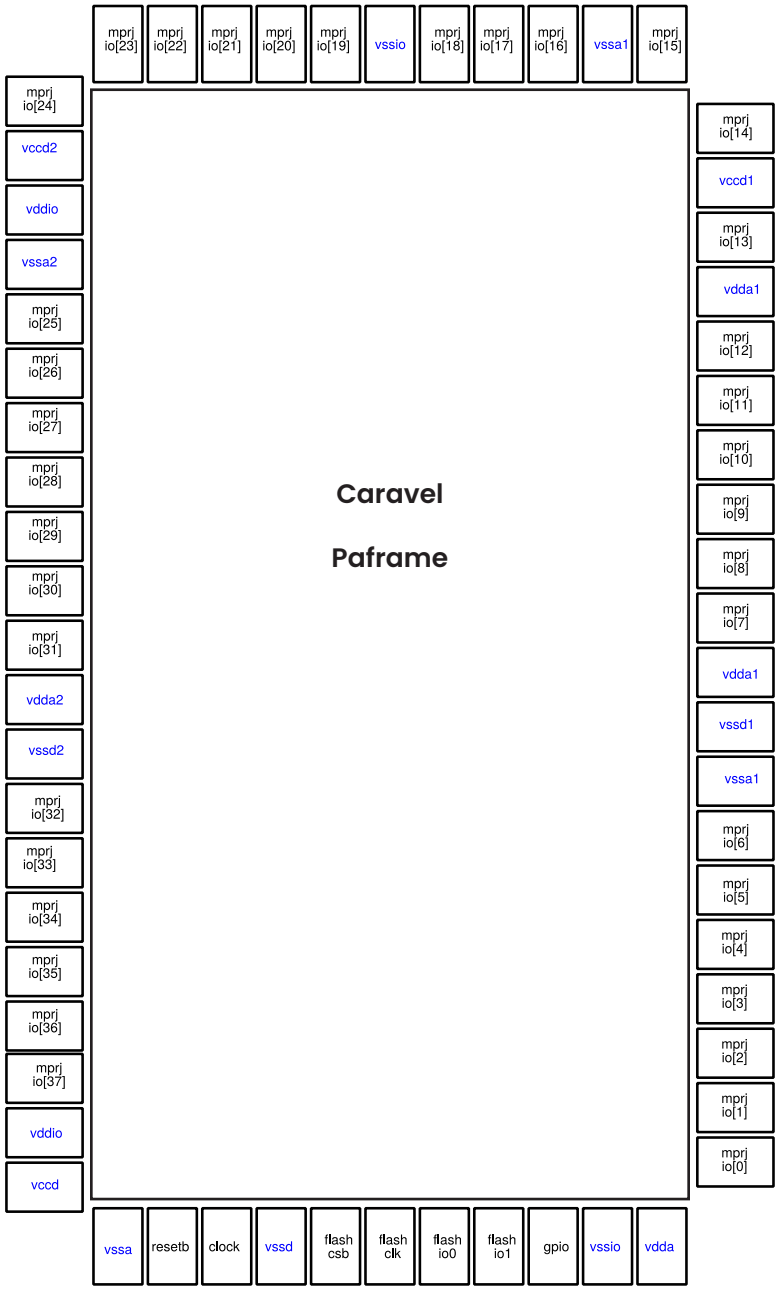
Package as viewed from the bottom.

Standard package: WLCSP (bump bond)
Bump pitch: 0.5mm
Package size: 3.2mm × 5.3mms

5.3. Bare die



Caravel padframe dimensions = 3.588 mm × 5.188 mm
Caravel die dimensions = 3.60 mm x 5.20 mm


mprj io[23]
mprj io[22]
mprj io[21]
mprj io[20]
mprj io[19]
vssio
mprj io[18]
mprj io[17]
mprj io[16]
vssa1
mprj io[15]
mprj io[24]
vccd2
vddio
vssa2
mprj io[25]
mprj io[26]
mprj io[27]
mprj io[28]
mprj io[29]
mprj io[30]
mprj io[31]
vdda2
vssd2
mprj io[32]
mprj io[33]
mprj io[34]
mprj io[35]
mprj io[36]
mprj io[37]
vddio
vccd
Caravel
Paframe
mprj io[14]
vccd1
mprj io[13]
vdda1
mprj io[12]
mprj io[11]
mprj io[10]
mprj io[9]
mprj io[8]
mprj io[7]
vdda1
vssd1
vssa1
mprj io[6]
mprj io[5]
mprj io[4]
mprj io[3]
mprj io[2]
mprj io[1]
mprj io[0]
vssa
resetb
clock
vssd
flash csb
flash clk
flash io0
flash io1
gpio
vssio
vdda

5.4. Pinout

Pin Name	Pin No (QFN)	Pin No (WCSP)		Pin Name	Pin No (QFN)	Pin No (WCSP)
vssa	1	C5,C6,D5,D6		mprj_io[2] / SDI	33	F9
mprj_io[25]	2	A3		mprj_io[3] / CSB	34	E9
mprj_io[26]	3	B4		mprj_io[4] / SCK	35	F8
mprj_io[27]	4	A4		mprj_io[5] / ser_rx	36	E7
mprj_io[28]	5	B5		mprj_io[6] / ser_tx	37	F7
mprj_io[29]	6	A5		**vssa1**	38	E6
mprj_io[30]	7	B6		**vssd1**	39	F6
mprj_io[31]	8	A6		**vdda1**	40	D4
vdda2	9	C7		mprj_io[7] / irq	41	E5
vssd2	10	B7		mprj_io[8]	42	F5
mprj_io[32] / spi_sck	11	A7		mprj_io[9]	42	E4
mprj_io[33] / spi_csb	12	C8		mprj_io[10]	44	F4
mprj_io[34] / spi_sdi	13	B8		mprj_io[11]	45	E3
mprj_io[35] / spi_sdo	14	A8		mprj_io[12]	46	F3
mprj_io[36]	15	B9		**vdda1**	47	D4
mprj_io[37]	16	A9		mprj_io[13]	48	D3
vddio	17	C4		**vccd1**	49	F2
vccd	18	A10		mprj_io[14]	50	E2
n/c	19	--		mprj_io[15]	51	F1
vssa	20	C5,C6,D5,D6		**vssa1**	52	E6
resetb	21	B10		mprj_io[16]	53	E1
clock	22	C9		mprj_io[17]	54	D2
vssd	23	C5,C6,D5,D6		mprj_io[18]	55	D1
flash_csb	24	C10		**vssio**	56	C5,C6,D5,D6
flash_clk	25	D8		mprj_io[19]	57	C1
flash_io0	26	D9		mprj_io[20]	58	C2
flash_io1	27	D10		mprj_io[21]	59	B1

Pin Name	Pin No (QFN)	Pin No (WCSP)		Pin Name	Pin No (QFN)	Pin No (WCSP)
gpio	28	E10		mprj_io[22]	60	B2
vssio	29	C5,C6,D5,D6		mprj_io[23]	61	A1
vdda	30	C5,C6,D5,D6		mprj_io[24]	62	C3
mprj_io[0] / JTAG	31	D7		**vccd2**	63	A2
mprj_io[1] / SDO	32	E9		vddio	64	C4

6. Ordering Information

Caravel is part of the chipIgnite solution for Efabless. More information regarding chipIgnite can be found at:

www.efabless.com/chipignite

To get started with creating a project, please see the following library of video get setup, create and develop a project, and submit it to Efabless for prototype fabrication.

www.efabless.com/getting-started

7. License