



SORBONNE UNIVERSITÉ

LIP6 Laboratory

CORIOLIS

User's Guide

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Credits & License

HURRICANE Rémy ESCASSUT & Christian MASSON
ETESIAN Gabriel GOUVINE
STRATUS Sophie BELLOEIL
KATANA (global) Damien DUPUIS
KATANA (detailed), UNICORN Jean-Paul CHAPUT

The HURRICANE data-base is copyright© BULL 2000-2019 and is released under the terms of the LGPL license. All other tools are copyright© UPMC 2008-2018, SORBONNE UNIVERSITÉ 2018-2019 and released under the GPL license.

Others important contributors to CORIOLIS are Christophe ALEXANDRE, Roselyne CHOTIN, Hugo CLEMENT, Marek SROKA and Wu YIFEI.

The KATANA router makes use of the FLUTE software, which is copyright© Chris C. N. CHU from the Iowa State University (<http://home.eng.iastate.edu/~cnchu/>).

Release Notes

Release 1.0.1475

This is the first preliminary release of the CORIOLIS 2 framework.

This release mainly ships the global router KNIK and the detailed router KITE. Together they aim to replace the ALLIANCE NERO router. Unlike NERO, KITE is based on an innovating routing modeling and ad-hoc algorithm. Although it is released under GPL license, the source code will be available later.

Contents of this release:

1. A graphical user interface (viewer only).
2. The KNIK global router.
3. The KITE detailed router.

Supported input/output formats:

- ALLIANCE **vst** (netlist) & **ap** (physical) formats.
- Even if there are some references to the CADENCE LEFDEF format, its support is not included because it depends on a library only available to SI2 affiliated members.

Release 1.0.1963

Release 1963 is alpha. All the tools from CORIOLIS 1 have been ported into this release.

Contents of this release:

1. The STRATUS netlist capture language (GENLIB replacement).
2. The MAUKA placer (still contains bugs).
3. A graphical user interface (viewer only).
4. The KNIK global router.
5. The KITE detailed router.
6. Partially implemented python support for configuration files (alternative to XML).
7. A documentation (imcomplete/obsoleted in HURRICANE's case).

Release 1.0.2049

Release 2049 is Alpha.

Changes of this release:

1. The HURRICANE documentation is now accurate. Documentation for the Cell viewer and CRLCORE has been added.
2. More extensive Python support for all the components of CORIOLIS.
3. Configuration is now completely migrated under Python. XML loaders can still be used for compatibility.
4. The `cgt` main has been rewritten in Python.

Release v2.0.1

1. Migrated the repository from `svn` to `git`, and release complete sources. As a consequence, we drop the distribution packaging support and give public read-only access to the repository.
2. Deep rewrite of the KATABATIC database and KITE detailed router, achieve a speedup factor greater than 20...

Release v2.1

1. Replace the old simulated annealing placer MAUKA by the analytical placer ETESIAN and its legalization and detailed placement tools.
2. Added a Blif format parser to process circuits generated by the Yosys and ABC logic synthesizers.
3. The multiple user defined configuration files are now grouped under a common hidden (dot) directory `.coriolis2` and the file extension is back from `.conf` to `.py`.

Release v2.2

1. Added JSON import/export of the whole Hurricane DataBase. Two save mode are supported: *Cell* mode (standalone) or *Blob* mode, which dump the whole design down and including the standard cells.

Release v2.3

1. Reverts to a more standard organisation of the branches. `devel_anabatic` is closed and we go on with `master` (stable version) and `devel`.
2. Makes KATANA the default global & detailed router. Put KNIK & KITE in the obsolete menus.
3. Finally makes use of PYQT4 widgets. Seems to integrate without problems with the CORIOLIS own QT widget. The drawback is that to build against QT 5 needs adjustment from the user.
4. Improved support for whole chip management. The outer part of the chip containing the pad is decoupled from the core. This allows to cleanly separate real pads from the foundry from a symbolic core. But this does not preclude other combinations as fully symbolic or fully real.

To perform the separation, an intermediate hierarchical level `corona` between chip and core has been introduced.

Release v2.4

1. Complete rewrite of the initialisation system. No longer use "configuration like" files with various list of items. Now the configuration is supplied under the form of PYTHON modules to be imported as the user see fit.
2. Clean separation between NDA protected parts and free ones. Now all the NDA related components are put under one separated tree, whether they are configuration files or PYTHON plugins, so that they be can easily by exported.
3. In ANABATIC & KATANA better accuracy at how obstacles decrease the edges capacities of the GCells. Reduce the edge capacity of a GCell according to it's inner cluttering (that is, it's number of terminals). Change of semantics for `katana.hReservedLocal` and `katana.vReservedLocal` parameters.

Complete Design Flow & Examples

While CORIOLIS can be used stand-alone, it is in fact part of a more complete design flow build upon YOSYS and ALLIANCE. In addition, a set of demos and examples are supplied in the repository `alliance-check-toolkit`.

- YOSYS : <http://www.clifford.at/yosys/>
An **rpm** packaged version is available here:
https://ftp.lip6.fr/pub/linux/distributions/slsoc/soc/7/addons/x86_64/repoview/yosys.html
- Alliance : <https://www-soc.lip6.fr/equipe-cian/logiciels/alliance/>
- `alliance-check-toolkit` **git** repository:
<https://www-soc.lip6.fr/git/alliance-check-toolkit.git/>

Installation



Note

As the sources are being released, the binary packaging is dropped. You may still find (very) old versions here: <http://asim.lip6.fr/pub/coriolis/2.0>.

In a nutshell, building source consists in pulling the **git** repository then running the **ccb** installer.



Note

The documentation is already generated and committed in the **git** tree. You may not install the additional prerequisites for the documentation. By default the documentation is not generated, just installed by **ccb**. If you really want to re-generate it, add the `--doc` flag to **ccb**.

Main building prerequisites:

- cmake
- C++11-capable compiler
- BFD library (provided through `binutils`).
- **RapidJSON**
- python2.7
- boost
- libxml2
- bzip2
- yacc & lex
- Qt 4 or Qt 5
- PyQt 4 or PyQt 5
- Qwt 6

Building documentation prerequisites:

- doxygen

- latex
- python-docutils (for reStructuredText)

The following libraries get directly bundled with CORIOLIS:

- LEF/DEF (from [Sl2](#))
- FLUTE (from [Chris C. N. Chu](#))

For other distributions, refer to their own packaging system.

Cross Dependencies Issues

There is a difficult tangle of dependencies between PYTHON, QT, QWT and PYQT, the requirements are:

- A PYTHON 2.7.
- QT, either 4 or 5.
- QWT version 6, compiled against the relevant QT version.
- PYQT, version 4 or 5, according to the chosen QT.

Problems arise because:

- Under RHEL 7 or clones, there is no compatible PYQT5 build compatible with their QT 5 version (we fall short of one minor, they provides QT 5.9 were we need at least QT 5.10). So we have to stick to QT 4 on those platforms.

Fortunately we can build a QWT 6 with QT 4.

- Under DEBIAN or UBUNTU there is no QWT 6 build against QT 4, so we have to use QT 5 and PYQT 5.

Fixed Directory Tree

In order to simplify the work of the **ccb** installer, the source, build and installation tree is fixed. To successfully compile CORIOLIS you must follow it exactly. The tree is relative to the home directory of the user building it (note `~/` or `$HOME/`). Only the source directory needs to be manually created by the user, all others will be automatically created either by **ccb** or the build system.

Sources	
Sources root under git	~/coriolis-2.x/src ~/coriolis-2.x/src/coriolis
Architecture Dependant Build	
Linux, SL 7, 64b Linux, SL 6, 32b Linux, SL 6, 64b Linux, Fedora, 64b Linux, Fedora, 32b FreeBSD 8, 32b FreeBSD 8, 64b Windows 7, 32b Windows 7, 64b Windows 8.x, 32b Windows 8.x, 64b	~/coriolis-2.x/Linux.el7_64/Release.Shared/build/<tool> ~/coriolis-2.x/Linux.slsoc6x/Release.Shared/build/<tool> ~/coriolis-2.x/Linux.slsoc6x_64/Release.Shared/build/<tool> ~/coriolis-2.x/Linux.fc_64/Release.Shared/build/<tool> ~/coriolis-2.x/Linux.fc/Release.Shared/build/<tool> ~/coriolis-2.x/FreeBSD.8x.i386/Release.Shared/build/<tool> ~/coriolis-2.x/FreeBSD.8x.amd64/Release.Shared/build/<tool> ~/coriolis-2.x/Cygwin.W7/Release.Shared/build/<tool> ~/coriolis-2.x/Cygwin.W7_64/Release.Shared/build/<tool> ~/coriolis-2.x/Cygwin.W8/Release.Shared/build/<tool> ~/coriolis-2.x/Cygwin.W8_64/Release.Shared/build/<tool>
Architecture Dependant Install	
Linux, SL 6, 32b	~/coriolis-2.x/Linux.slsoc6x/Release.Shared/install/
FHS Compliant Structure under Install	
Binaries Libraries (Python) Include by tool Configuration files Doc, by tool	.../install/bin .../install/lib .../install/include/coriolis2/<project>/<tool> .../install/etc/coriolis2/ .../install/share/doc/coriolis2/en/html/<tool>

**Note**

Alternate build types: the `Release.Shared` means an optimized build with shared libraries. But there are also available `Static` instead of `Shared` and `Debug` instead of `Release` and any combination of them. `Static` does not work because I don't know yet to mix statically linked binaries and Python modules (which must be dynamic).

Building Coriolis

The actively developed branch

The **devel_anabatic** branch is now closed and we go back to a more classical scheme where **master** is the stable version and **devel** the development one.

The CORIOLIS **git** repository is <https://www-soc.lip6.fr/git/coriolis.git>

**Note**

Again, the **devel_anabatic** branch is now closed. Please revert to **devel** or **master**.

**Note**

Under RHEL 7 or clones, they upgraded their version of QT 4 (from 4.6 to 4.8) so the *diagonal line* bug no longer occurs. So we can safely use the default system QT again.

Installing on REDHAT or compatible distributions

1. Install or check that the required prerequisites are installed :

```
dummy@lepka:~> yum install -y git cmake bison flex gcc-c++ libstdc++-devel \
    binutils-devel \
    boost-devel boost-python boost-filesystem \
    boost-regex boost-wave \
    python-devel libxml2-devel bzip2-devel \
    qt-devel qwt-devel
```

Note, that the `Qwt` packages are directly available from the standart distribution when using QT 4.

2. Install the unpackaged prerequisites. Currently, only **RapidJSON**.

```
dummy@lepka:~> mkdir -p ~/coriolis-2.x/src/support
dummy@lepka:support> cd ~/coriolis-2.x/src/support
dummy@lepka:support> git clone http://github.com/miloyip/rapidjson
```

3. Create the source directory and pull the **git** repository:

```
dummy@lepka:~> mkdir -p ~/coriolis-2.x/src
dummy@lepka:src> cd ~/coriolis-2.x/src
dummy@lepka:src> git clone https://www-soc.lip6.fr/git/coriolis.git
```

4. Build & install:

```
dummy@lepka:src> cd coriolis
dummy@lepka:coriolis> git checkout devel
dummy@lepka:coriolis> ./bootstrap/ccb.py --project=support \
    --project=coriolis \
    --make="-j4 install"
```

Note

Pre-generated documentation will get installed by the previous command. Only if you did made modifications to it you need to regenerate it with:



```
dummy@lepka:coriolis> ./bootstrap/ccb.py --project=support \
    --project=coriolis \
    --doc --make="-j1 install"
```

We need to perform a separate installation of the documentation because it does not support to be generated with a parallel build. So we compile & install in a first stage in `-j4` (or whatever) then we generate the documentation in `-j1`

Under RHEL6 or clones, you must build using the **devtoolset**, the version is to be given as argument:

```
dummy@lepka:coriolis> ./bootstrap/ccb.py --project=coriolis \
    --devtoolset=8 --make="-j4 install"
```

If you want to use Qt 5 instead of Qt 4, modify the previous steps as follows:

- At **step 1**, do not install the QT 4 related development package (`qt4-devel`), but instead:

```
dummy@lepka:~> yum install -y qt5-qtbase-devel qt5-qtsvg-devel
```

The package `qwt-qt5-devel` and it's dependency `qwt-qt5` are not provided by any standard repository (like EPEL). You may download them from the [LIP6 Addons Repository](#). Then run:

```
dummy@lepka:~> yum localinstall -y qwt-qt5-6.1.2-4.fc23.x86_64.rpm \
qwt-qt5-6.1.2-4.fc23.x86_64.rpm # Qwt for
```

- At **step 4**, add a `--qt5` argument to the `ccb.py` command line.
- The PYTHON scripts that make use of PYQT in `crlcore` and `cumulus` must be edited to import `PyQt5` instead of `PtQt4` (should find a way to automatically switch between the two of them).

The complete list of **ccb** functionalities can be accessed with the `--help` argument. It also may be run in graphical mode (`--gui`).

Building a Debug Enabled Version

The `Release.Shared` default version of the CORIOLIS is built stripped of symbols and optimized so that it makes analysing a core dump after a crash difficult. In the (unlikely) case of a crash, you may want to build, alongside the optimized version, a debug one which allows forensic examination by **gdb** (or **valgrind** or whatever).

Run again `ccb.py`, adding the `--debug` argument:

```
dummy@lepka:coriolis> ./bootstrap/ccb.py --project=support \
--project=coriolis \
--make="-j4 install" --debug
```

As `cgt` is a PYTHON script, the right command to run **gdb** is:

```
dummy@lepka:work> gdb python core.XXXX
```

Installing on DEBIAN 9, UBUNTU 18 or compatible distributions

First, install or check that the required prerequisites are installed :

```
dummy@lepka:~> sudo apt install -y build-essential binutils-dev
git cmake bison flex gcc python-dev
libboost-all-dev libboost-python-dev
libbz2-dev libxml2-dev rapidjson-dev libbz2-dev
qtbase5-dev libqt5svg5-dev libqwt-qt5-dev
python-pyqt5
doxygen dviPNG graphviz python-sphinx
texlive-fonts-extra texlive-lang-french
```

Second step is to create the source directory and pull the **git** repository:

```
dummy@lepka:~> mkdir -p ~/coriolis-2.x/src
dummy@lepka:src> cd ~/coriolis-2.x/src
dummy@lepka:src> git clone https://www-soc.lip6.fr/git/coriolis.git
```

Third and final step, build & install:

```
dummy@lepka:src> cd coriolis
dummy@lepka:coriolis> git checkout devel
dummy@lepka:coriolis> ./bootstrap/ccb.py --project=coriolis --qt5 \
--make="-j4 install"
```

Additional Requirement under MacOS

CORIORIS makes use of the `boost : :python` module, but the MACPORTS `boost` seems unable to work with the PYTHON bundled with MacOS. So you have to install both of them from MACPORTS:

```
dummy@macos:~> port install boost +python27
dummy@macos:~> port select python python27
dummy@macos:-> export DYLD_FRAMEWORK_PATH=/opt/local/Library/Frameworks
```

The last two lines tell MacOS to use the PYTHON from MACPORTS and *not* from the system. Then proceed with the generic install instructions.

Packaging Coriolis

Packager should not use `ccb`, instead `bootstrap/Makefile.package` is provided to emulate a top-level `autotool` makefile. Just copy it in the root of the CORIORIS git repository (`~/corriolis-2.x/src/coriolis/`) and build.

Slightly outdated packaging configuration files can also be found under `bootstrap/`:

- `bootstrap/coriolis2.spec.in` for `rpm` based distributions.
- `bootstrap/debian` for DEBIAN based distributions.

Hooking up into ALLIANCE

CORIORIS relies on ALLIANCE for the cell libraries. So after installing or packaging, you must configure it so that it can found those libraries.

The easiest way is to setup the ALLIANCE environment (i.e. sourcing `.../etc/profile.d/alc_env.{sh,csh}`) **before** setting up CORIORIS environment (see the next section). To understand how CORIORIS find/setup ALLIANCE you may have look to the *Configuration and User's Settings* section.

Setting up the Environment (coriolisEnv.py)

To simplify the tedious task of configuring your environment, a helper is provided in the `bootstrap` source directory (also installed in the directory `.../install/etc/coriolis2/`):

```
~/corriolis-2.x/src/coriolis/bootstrap/coriolisEnv.py
```

Use it like this:

```
dummy@lepka:~> eval `~/corriolis-2.x/src/coriolis/bootstrap/coriolisEnv.py`
```



Note

Do not call that script in your environment initialisation. When used under RHEL6 or clones, it needs to be run in the `devtoolset` environment. The script then launch a new shell, which may cause an infinite loop if it's called again in, say `~/ .bashrc`. Instead you may want to create an alias:

```
alias c2r='eval "`~/corriolis-2.x/src/coriolis/bootstrap/coriolisEnv.py`'
```

Coriolis Configuration & Initialisation

General Software Architecture

CORIORIS has been built with respect of the classical paradigm that the computational intensive parts have been written in C++, and almost everything else in PYTHON. To build the PYTHON interface we used two methods:

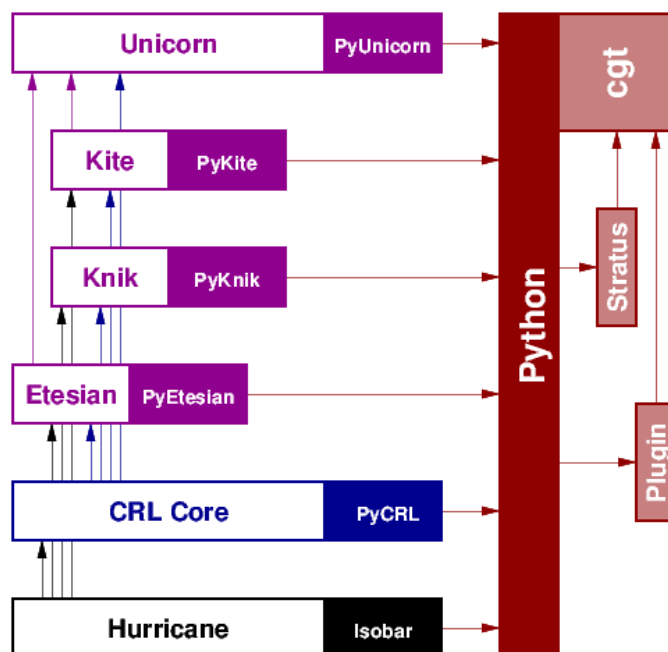
- For self-contained modules `boost : :python` (mainly in `v1sisapd`).

- For all modules based on HURRICANE, we created our own wrappers due to very specific requirements such as shared functions between modules or C++/PYTHON secure bi-directional object deletion.



Note

Python Documentation: Most of the documentation is related to the C++ API and implementation of the tools. However, the PYTHON bindings have been created so they mimic *as closely as possible* the C++ interface, so the documentation applies to both languages with only minor syntactic changes.



Configuration & User's Settings

All configurations files are shipped under the form of PYTHON modules. They are to be loaded through `import` statements. The user's configuration files must be put in a `./coriolis2/` directory under the working directory. It must be made a PYTHON module so it must contains a `__init__.py` file (kept empty most of the time). And as they are true PYTHON files, you may use in them any valid code you see fit.

If no user configuration files are present, CORIOLIS will use the default `symbolic.cmos` technology which matches the ALLIANCE symbolic default one.

Contents of the user's configuration directory `./coriolis2/`:

File	Contents/Meaning
<code>./coriolis2/__init__.py</code>	Mandatory. Tells PYTHON this directory <i>is</i> a module. Can be left empty
<code>./coriolis2/settings.py</code>	Mandatory. The user's settings, it must setup the technology intended for use and perform any configuration variable settings
<code>./coriolis2/ioring.py</code>	Optional. Define how the I/O pads are to be placed on the periphery of the chip along the chip and core sizes
<code>./coriolis2/katana.py</code>	Optional. Hook file for KATANA, run just after the tool has been created for a <code>Cell</code> . Mostly to setup <code>Nets</code> to be traced

For example, to use Mosis 180nm, you can put in your `./coriolis2/setting.py`:

```
# -*- Mode:Python -*-

import node180.scn6m_deep_09
```

A Comprehensive Example of `./coriolis2/setting.py`

```
import os
import Cfg
import Viewer
import CRL
import node180.scn6m_deep_09
from helpers import l, u, n

allianceTop = None
if os.environ.has_key('ALLIANCE_TOP'):
    allianceTop = os.environ['ALLIANCE_TOP']
    if not os.path.isdir(allianceTop):
        allianceTop = None

if not allianceTop: allianceTop = '/soc/alliance'

Cfg.Configuration.pushDefaultPriority( Cfg.Parameter.Priority.UserFile )

Viewer.Graphics.setStyle( 'Alliance.Classic [black]' )

cellsTop = allianceTop+'/cells'

# Alliance related settings.
af = CRL.AllianceFramework.get()
env = af.getEnvironment()

env.setScale_X          ( 100 )
env.setCATALOG          ( 'CATAL' )
env.setIN_LO            ( 'vst' )
env.setIN_PH            ( 'ap' )
env.setOUT_LO           ( 'vst' )
env.setOUT_PH           ( 'ap' )
env.setPOWER            ( 'vdd' )
env.setGROUND           ( 'vss' )
env.setCLOCK            ( '.*ck.*|.nck.*' )
env.setBLOCKAGE         ( 'blockage[Nn]et.*' )
env.setPad              ( '.*_mpx$' )

env.setWORKING_LIBRARY ( '.' )
env.addSYSTEM_LIBRARY ( library=cellsTop+'/nsxlib', mode=CRL.Environment.Append
env.addSYSTEM_LIBRARY ( library=cellsTop+'/mpxlib', mode=CRL.Environment.Append

# Misc. setting parameters.
Cfg.getParamBool ( 'misc.logMode' ) .setBool ( False
Cfg.getParamBool ( 'misc.verboseLevel1' ) .setBool ( True
Cfg.getParamBool ( 'misc.verboseLevel2' ) .setBool ( True

# P&R related parameters.
Cfg.getParamString ( 'anabatic.routingGauge' ) .setString ( 'msxlib4'
```

```

Cfg.getParamString ( 'anabatic.topRoutingLayer' ) .setString ( 'METAL4'
Cfg.getParamInt ( 'katana.hTracksReservedLocal' ) .setInt ( 6
Cfg.getParamInt ( 'katana.vTracksReservedLocal' ) .setInt ( 3

```

```
Cfg.Configuration.popDefaultPriority()
```

The example above shows the user's configuration file, with all the available settings for ALLIANCE and a small subset for other tools. Some remarks about this file:

- The `Cfg.Configuration.pushDefaultPriority()` and `Cfg.Configuration.popDefaultPriority()` statements are there so the value sets by the user will not be overridden by system ones even if they are setup afterwards. This priority system is introduced so the various configuration files could be loaded in out of order.
- The `Viewer.Graphics.setStyle()` allows you to choose the look of your liking from the start.
- For ALLIANCE, the user does not need to redefine all the settings, just the one he wants to change. In most of the cases, the `addSYSTEM_LIBRARY()`, the `setWORKING_LIBRARY()` and the special net names (at this point there is not much alternatives for the others settings).
- `addSYSTEM_LIBRARY()` adds a directory to the library search path. Each library entry will be added to the search path according to the second parameter:
 - **CRL.Environment::Append:** append to the search path.
 - **CRL.Environment::Prepend:** insert in head of the search path.
 - **CRL.Environment::Replace:** look for a library of the same name and replace it, without changing the search path order. If no library of that name already exists, it is appended.

A library is identified by its name, this name is the last component of the path name. For instance: `/soc/alliance/sxlib` will be named `sxlib`. Implementing the ALLIANCE specification, when looking for a *Cell* name, the system will browse sequentially through the library list and returns the first *Cell* whose name match.

- For `setPOWER()`, `setGROUND()`, `setCLOCK()` and `setBLOCKAGE()` net names, a regular expression (GNU regex) is expected.
- For other tools parameters, just use getter and setter according to their types:

Type	Getter/Setter
Bool	<code>Cgt.getParamBool('name').setBool(True)</code>
Int	<code>Cgt.getParamInt('name').setBool(12)</code>
Enumerate	<code>Cgt.getParamEnumerate('name').setBool(12)</code>
Double	<code>Cgt.getParamDouble('name').setDouble(254.5)</code>
Percentage	<code>Cgt.getParamPercentage('name').setPercentage(75.0)</code>
String	<code>Cgt.getParamString('name').setString('machin')</code>

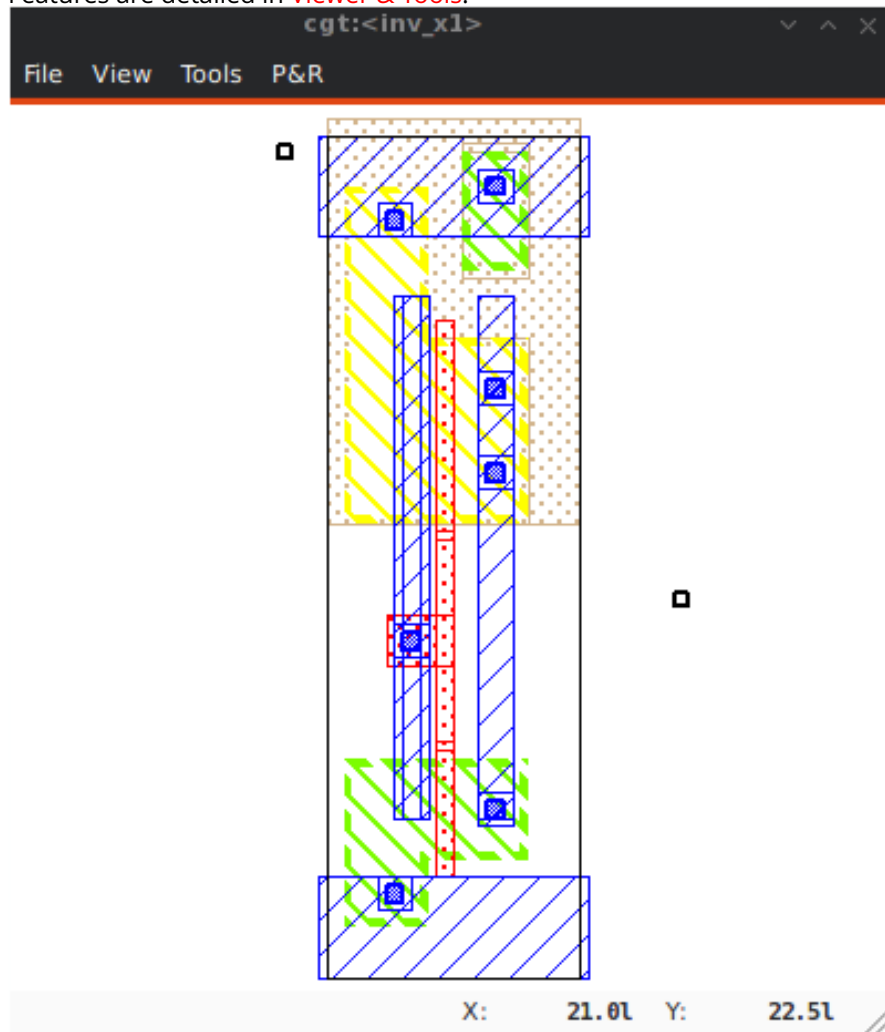
Lists of the configurable parameters of most interest to the user are given in [Viewer & Tools](#).

CGT - The Graphical Interface

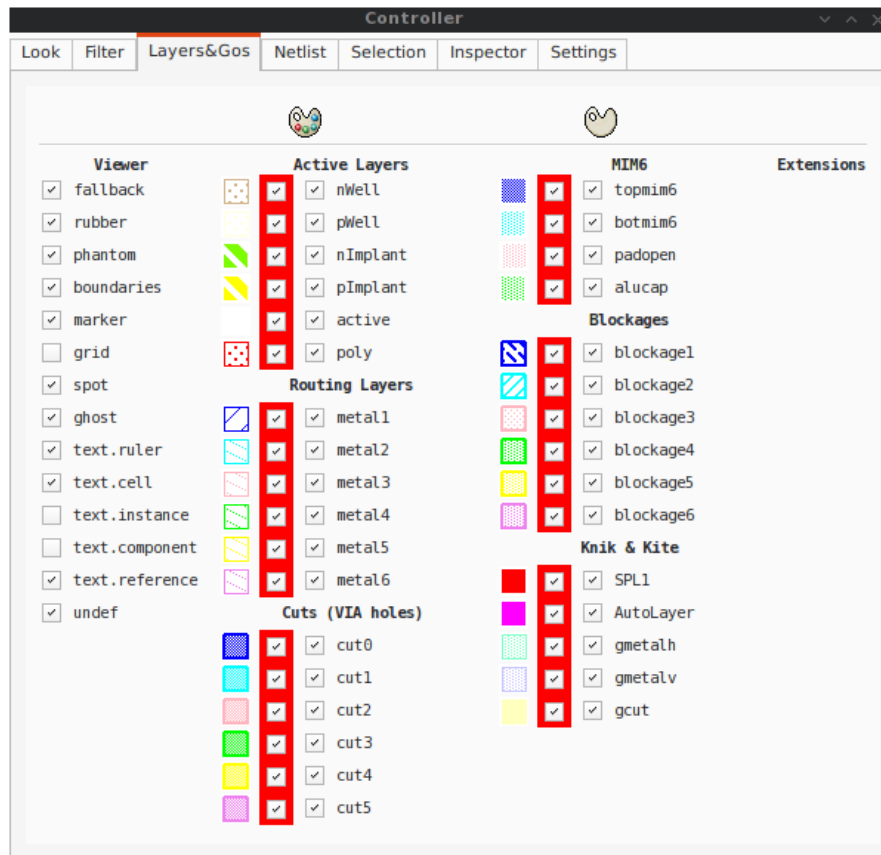
The CORIOLIS graphical interface is split up into two windows.

- The **Viewer**, with the following features:
 - Basic load/save capabilities.
 - Displays the current working cell. Could be empty if the design is not yet placed.
 - Executes Stratus Scripts.
 - Menu to run the tools (placement, routage).

Features are detailed in [Viewer & Tools](#).



- The **Controller**, which allows to:
 - Tweak what is displayed by the *Viewer*. Through the *Look*, *Filter* and *Layers&Gos* tabs.
 - Browse the *netlist* with eponym tab.
 - Show the list of selected objects (if any) with *selection*
 - Walk through the Database, the Cell or the Selection with *Inspector*. This is an advanced feature, reserved for experimented users.
 - The tab *Settings* which gives access to all the settings. They are closely related to Configuration & Initialisation.



Viewer & Tools

STRATUS Netlist Capture

STRATUS is the replacement for GENLIB procedural netlist capture language. It is designed as a set of PYTHON classes, and comes with it's own documentation ([Stratus Documentation](#))

The HURRICANE Data-Base

The ALLIANCE flow is based on the MBK data-base, which has one data-structure for each view. That is, **Lofig** for the *logical* view and **Phfig** for the *physical* view. The place and route tools were responsible for maintaining (or not) the coherency between views. Reflecting this weak coupling between views, each one was stored in a separate file with a specific format. The *logical* view is stored in a **vst** file in VHDL format and the *physical* in an **ap** file in an ad-hoc format.

The CORIOLIS flow is based on the HURRICANE data-base, which has a unified structure for *logical* and *physical* view. That data structure is the *Cell* object. The *Cell* can have any state between pure netlist and completely placed and routed design. Although the memory representation of the views has deeply changed we still use the ALLIANCE files format, but they now really represent views of the same object. The point is that one must be very careful about view coherency when going to and from CORIOLIS.

As for the second release, CORIOLIS can be used only for three purposes :

- **Placing a design**, in which case the *netlist* view must be present.
- **Routing a design**, in that case the *netlist* view and the *layout* view must be present and *layout* view must contain a placement. Both views must have the same name. When saving the routed design, it is advised to change the design name otherwise the original unrouted placement in the *layout* view will be overwritten.

- **Viewing a design**, the *netlist* view must be present, if a *layout* view is present it still must have the same name but it can be in any state.

Synthesizing and loading a design

COROLIS supports several file formats. It can load all file format from the ALLIANCE toolchain (.ap for layout, behavioural and structural vhdl .vbe and .vst), BLIF netlist format as well as benchmark formats from the ISPD contests.

It can be compiled with LEF/DEF support, although it requires acceptance of the SI2 license and may not be compiled in your version of the software.

Synthesis under Yosys You can create a BLIF file from the Yosys synthesizer, which can be imported under Coriolis. Most libraries are specified as a .lib liberty file and a .lef LEF file. Yosys opens most .lib files with minor modifications, but LEF support in Coriolis relies on SI2. If Coriolis hasn't been compiled against it, the library is given in ALLIANCE .ap format. **Some free libraries** already provide both .ap and .lib files.

Once you have installed a common library under Yosys and Coriolis, just synthesize your design with Yosys and import it (as Blif without the extension) under Coriolis to perform place&route.

Synthesis under Alliance ALLIANCE is an older toolchain but has been extensively used for years. Coriolis can import and write Alliance designs and libraries directly.

Etesian -- Placer

The ETESIAN placer is a state of the art (as of 2015) analytical placer. It is within 5% of other placers' solutions, but is normally a bit worse than ePlace. This COROLIS tool is actually an encapsulation of COLOQUINTE which is the placer.



Note

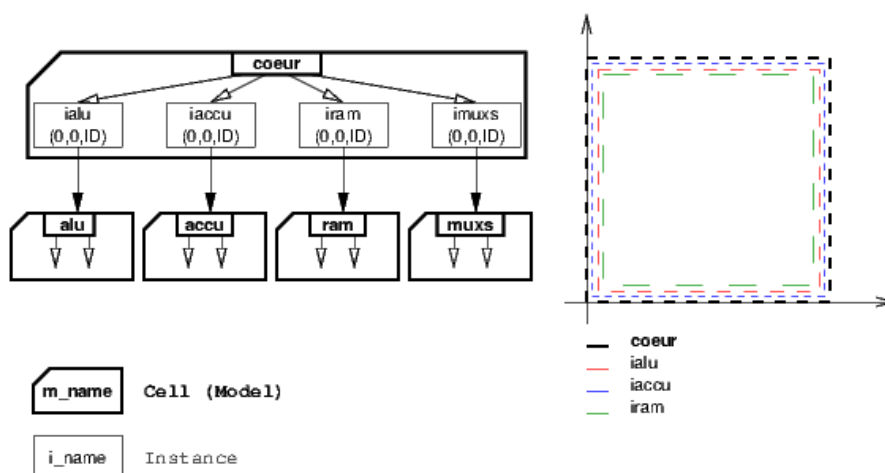
Instance Uniquification: a same logical instance cannot have two different placements. So, if you don't supply a placement for it, it will be uniquified (cloned) and you will see the copy files appears on disk upon saving.

Hierarchical Placement

The placement area is defined by the top cell abutment box.

When placing a complete hierarchy, the abutment boxes of the cells (models) other than the top cell are set identical to the one of the top cell and their instances are all placed at position (0, 0, ID). That is, all the abutments boxes, whatever the hierarchical level, define the same area (they are exactly superposed).

We choose this scheme because the placer will see all the instances as virtually flattened, so they can be placed anywhere inside the top-cell abutment box.



Computing the Placement Area

The placement area is computed using the `etesian.aspectRatio` and `etesian.spaceMargin` parameters only if the top-cell has an empty abutment box. If the top-cell abutment box has to be set, then it is propagated to all the instances models recursively.

Resetting the Placement

Once a placement has been done, the placer cannot reset it (will be implemented later). To perform a new placement, you must restart `cgt`. In addition, if you have saved the placement on disk, you must erase any `.ap` file, which are automatically reloaded along with the netlist (`.vst`).

Limitations

Etesian supports standard cells and fixed macros. As for the Coriolis 2.1 version, it doesn't support movable macros, and you must place every macro beforehand. Timing and routability analysis are not included either, and the returned placement may be unroutable.

Etesian Configuration Parameters

Parameter Identifier	Type	Default
Etesian Parameters		
<code>etesian.aspectRatio</code>	Percentage	100
	Define the height on width H/W aspect ratio, can be comprised between 10 and 1000	
<code>etesian.spaceMargin</code>	Percentage	5
	The extra white space added to the total area of the standard cells	
<code>etesian.uniformDensity</code>	Bool	False
	Whether the cells will be spread evenly across the area or allowed to form denser clusters	
<code>etesian.effort</code>	Int	2
	Sets the balance between the speed of the placer and the solution quality	
<code>etesian.routingDriven</code>	Bool	False
	Whether the tool will try routing iterations and whitespace allocation to improve routability; to be implemented	
<code>etesian.graphics</code>	Int	2
	How often the display will be refreshed More refreshing slows the placer. <ul style="list-style-type: none"> • 1 shows both upper and lower bounds • 2 only shows lower bound results • 3 only shows the final results 	

Katana -- Global Router

The quality of KATANA global routing solutions are equivalent to those of FGR 1.0. For an in-depth description of KATANA algorithms, you may download the thesis of D. DUPUIS available from here-: [Knik Thesis](#) (KNIK has been rewritten as part of KATANA, the algorithms remains essentially the same).

The global router is now deterministic.

Katana -- Detailed Router

KATANA no longer suffers from the limitations of NERO. It can route big designs as its runtime and memory footprint is almost linear (with respect to the number of gates). It has successfully routed design of more than 150K gates.



Note

Slow Layer Assignment. Most of the time, the layer assignment stage is fast (less than a dozen seconds), but in some instances it can take more than a dozen *minutes*. This is a known bug and will be corrected in later releases.

After each run, KATANA displays a set of *completion ratios* which must all be equal to 100% or (NNNN+0) if the detailed routing has been successful. In the event of a failure, on a saturated design, you may tweak the three following configuration parameters:

1. `katana.hTrackReservedLocal`, the number of track reserved for local routing, that quantity is subtracted from the edge capacities (global routing) to give a sense of the cluttering inside the GCells.
2. `katana.vTrackReservedLocal`, same as above.
3. `etesian.spaceMargin`, increases the free area of the overall design so the routing density decrease.

The idea is to increase the horizontal and vertical local track reservation until the detailed router succeeds. But in doing so we make the task of the global router more and more difficult as the capacity of the edges decreases, and at some point it will fail too. So this is a balance.

Routing a design is done in four ordered steps:

1. Detailed pre-route **P&R** → **Step by Step** → **Detailed PreRoute**
2. Global routing **P&R** → **Step by Step** → **Global Route**
3. Detailed routing **P&R** → **Step by Step** → **Detailed Route**
4. Finalize routing **P&R** → **Step by Step** → **Finalize Route**

It is possible to supply to the router a complete wiring for some nets that the user wants to be routed according to a specific topology. The supplied topology must respect the building rules of the ANABATIC database (contacts must be, *terminals*, *turns*, *h-tee* & *v-tee* only). During the first step `Detailed Pre-Route` the router will solve overlaps between the segments, without making any dogleg. If no pre-routed topologies are present, this step may be omitted. Any net routed at this step is then fixed and become unmovable for the later stages.

After the detailed routing step the KATANA data-structure is still active (the Hurricane wiring is decorated). The finalize step performs the removal of the KATANA data-structure, and it is not advisable to save the design before that step.

You may visualize the density (saturation) of either the edges (global routing) or the GCells (detailed routing) until the routing is finalized. Special layers appear to that effect in the [The Layers&Go Tab](#).

Katana Configuration Parameters The ANABATIC parameters control the layer assignment step.

All the defaults value given below are from the default ALLIANCE technology (**cmos** and **SxLib** cell gauge/routing gauge).

Parameter Identifier	Type	Default
Anabatic Parameters		
anabatic.topRoutingLayer	String	METAL5
	Define the highest metal layer that will be used for routing (inclusive).	
anabatic.globalLengthThreshold	Int	1450
	This parameter is used by a layer assignment method which is no longer used (did not give good results)	
anabatic.saturateRatio	Percentage	80
	If $M(x)$ density is above this ratio, move up feedthru global segments up from depth x to $x+2$	
anabatic.saturateRp	Int	8
	If a GCell contains more terminals (RoutingPad) than that number, force a move up of the connecting segments to those in excess	
anabatic.globalIterations	Int	10
	The maximum number of iterations the global router will try to solve edges overload	
Katana Parameters		
katana.hTracksReservedLocal	Int	3
	To take account the tracks needed <i>inside</i> a GCell to build the <i>local</i> routing the capacities of the edges needs to be decreased. The decrease is computed by the GCell and cannot exceed this number (this is maximum). For better accuracy vertical and horizontal edges are distinguished	
katana.vTracksReservedLocal	Int	3
	cf. kite.hTracksReservedLocal	
katana.eventsLimit	Int	4000002
	The maximum number of segment displacements, this is a last ditch safety against infinite loop. It's perhaps a little too low for big designs	
katana.ripupCost	Int	3
	Differential introduced between two ripup costs to avoid a loop between two ripped up segments	
katana.strapRipupLimit	Int	16
	Maximum number of ripup for <i>strap</i> segments	
katana.localRipupLimit	Int	9
	Maximum number of ripup for <i>local</i> segments	
katana.globalRipupLimit	Int	5
	Maximum number of ripup for <i>global</i> segments, when this limit is reached, triggers topologic modification	

... continued on next page

Parameter Identifier	Type	Default
katana.longGlobalRipupLimit	Int	5
	Maximum number of ripup for <i>long global</i> segments, when this limit is reached, triggers topological modification	

Executing Python Scripts in Cgt

Python/Stratus scripts can be executed either in text or graphical mode.



Note

How Cgt Locates Python Scripts: `cgt` uses the Python `import` mechanism to load Python scripts. So you must give the name of your script without `.py` extension and it must be reachable through the `PYTHONPATH`. You may use the dotted module notation.

A Python/Stratus script must contain a function called `ScriptMain()` with one optional argument, the graphical editor into which it may be running (will be set to `None` in text mode). The Python interface to the editor (type: **CellViewer**) is limited to basic capabilities only.

Any script given on the command line will be run immediately *after* the initializations and *before* any other argument is processed.

For more explanation on Python scripts see [Python Interface to Coriolis](#).

Printing & Snapshots

Printing or saving into a PDF is fairly simple, just use the **File -> Print** menu or the `CTRL+P` shortcut to open the dialog box.

The print functionality uses exactly the same rendering mechanism as for the screen, being almost *WYSIWYG*. Thus, to obtain the best results it is advisable to select the `Coriolis.Printer` look (in the *Controller*), which uses a white background and well suited for high resolutions 32x32 pixels patterns

There is also two modes of printing selectable through the *Controller Settings -> Misc -> Printer/Snapshot Mode*:

Mode	DPI (approx.)	Intended Usage
Cell Mode	150	For single <code>Cell</code> printing or very small designs. Patterns will be bigger and more readable.
Design Mode	300	For designs (mostly composed of wires and cells outlines).






Note

The pdf file size Be aware that the generated PDF files are indeed only pixmaps. So they can grow very large if you select paper format above A2 or similar.

Saving into an image is subject to the same remarks as for PDF.

Memento of Shortcuts in Graphic Mode

The main application binary is `cgt`.

Category	Keys	Action
Moves	<div style="display: flex; flex-wrap: wrap; gap: 5px;"> <div style="border: 1px solid black; padding: 2px;">Up</div> <div style="border: 1px solid black; padding: 2px;">Down</div> <div style="border: 1px solid black; padding: 2px;">Left</div> <div style="border: 1px solid black; padding: 2px;">Right</div> </div>	Shifts the view in the according direction
Fit	<div style="border: 1px solid black; padding: 2px;">f</div>	Fits to the Cell abutment box
Refresh	<div style="border: 1px solid black; padding: 2px;">CTRL+L</div>	Triggers a complete display redraw
Goto	<div style="border: 1px solid black; padding: 2px;">g</div>	<i>aperture</i> is the minimum side of the area displayed around the point to go to. It's an alternative way of setting the zoom level
Zoom	<div style="border: 1px solid black; padding: 2px;">z</div> , <div style="border: 1px solid black; padding: 2px;">m</div>	Respectively zoom by a 2 factor and <i>unzoom</i> by a 2 factor
	 Area Zoom	You can perform a zoom to an area. Define the zoom area by <i>holding down the left mouse button</i> while moving the mouse.
Selection	 Area Selection	You can select displayed objects under an area. Define the selection area by <i>holding down the right mouse button</i> while moving the mouse.
	 Toggle Selection	You can toggle the selection of one object under the mouse position by pressing <div style="border: 1px solid black; padding: 2px;">CTRL</div> and pressing down <i>the right mouse button</i> . A popup list of what's under the position shows up into which you can toggle the selection state of one item.
	<div style="border: 1px solid black; padding: 2px;">S</div>	Toggle the selection visibility
Controller	<div style="border: 1px solid black; padding: 2px;">CTRL+I</div>	Show/hide the controller window. It's the Swiss Army Knife of the viewer. From it, you can fine-control the display and inspect almost everything in your design.
Rulers	<div style="border: 1px solid black; padding: 2px;">k</div> , <div style="border: 1px solid black; padding: 2px;">ESC</div>	One stroke on <div style="border: 1px solid black; padding: 2px;">k</div> enters the ruler mode, in which you can draw one ruler. You can exit the ruler mode by pressing <div style="border: 1px solid black; padding: 2px;">ESC</div> . Once in ruler mode, the first click on the <i>left mouse button</i> sets the ruler's starting point and the second click the ruler's end point. The second click exits automatically the ruler mode.
	<div style="border: 1px solid black; padding: 2px;">K</div>	Clears all the drawn rulers
Print	<div style="border: 1px solid black; padding: 2px;">CTRL+P</div>	Currently rather crude. It's a direct copy of what's displayed in pixels. So the resulting picture will be a little blurred due to anti-aliasing mechanism.
Open/Close	<div style="border: 1px solid black; padding: 2px;">CTRL+O</div>	Opens a new design. The design name must be given without path or extension.
	<div style="border: 1px solid black; padding: 2px;">CTRL+W</div>	Closes the current viewer window, but does not quit the application.
	<div style="border: 1px solid black; padding: 2px;">CTRL+Q</div>	<i>CTRL+Q</i> quits the application (closing all windows).

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Category	Keys	Action
Hierarchy	CTRL+Down	Goes one hierarchy level down. That is, if there is an <i>instance</i> under the cursor position, loads its <i>model</i> Cell in place of the current one.
	CTRL+Up	Goes one hierarchy level up. If we have entered the current model through CTRL+Down reloads the previous model (the one in which this model is instanciated).

Cgt Command Line Options

Appart from the obvious `--text` options, all can be used for text and graphical mode.

Arguments	Meaning
<code>-t --text</code>	Instructs cgt to run in text mode.
<code>-L --log-mode</code>	Disables the use of ANSI escape sequence on the tty . Useful when the output is redirected to a file.
<code>-c <cell> --cell=<cell></code>	The name of the design to load, without leading path or extention.
<code>-m <val> --margin=<val></code>	Percentage <i>val</i> of white space for the placer (ETESIAN).
<code>--events-limit=<count></code>	The maximal number of events after which the router will stop. This is mainly a failsafe against looping. The limit is set to 4 millions of iteration which should suffice to any design of 100K. gates. For bigger designs you may want to increase this limit.
<code>-G --global-route</code>	Runs the global router (KATANA).
<code>-R --detailed-route</code>	Runs the detailed router (KATANA).
<code>-s --save-design=<routed></code>	The design into which the routed layout will be saved. It is strongly recommanded to choose a different name from the source (unrouted) design.
<code>--stratus-script=<module></code>	Run the Python/Stratus script <code>module</code> . See Python Scripts in Cgt .

Some Examples :

- Run both global and detailed router, then save the routed design :

```
> cgt -v -t -G -R --cell=design --save-design=design_r
```

Miscellaneous Settings

Parameter Identifier	Type	Default
Verbosity/Log Parameters		
misc.info	Bool	False
	Enables display of <i>info</i> level message (cinfo stream)	
misc.bug	Bool	False
	Enables display of <i>bug</i> level message (cbug stream), messages can be a little scary	
misc.logMode	Bool	False
	If enabled, assumes that the output device is not a <i>tty</i> and suppresses any escape sequences	
misc.verboseLevel1	Bool	True
	First level of verbosity, disables level 2	
misc.verboseLevel2	Bool	False
	Second level of verbosity	
Development/Debug Parameters		
misc.minTraceLevel	Int	0
misc.maxTraceLevel	Int	0
	Displays trace information <i>between</i> those two levels (cdebug stream)	
misc.catchCore	Bool	False
	By default, cgt does not dump core. To generate one set this flag to True	

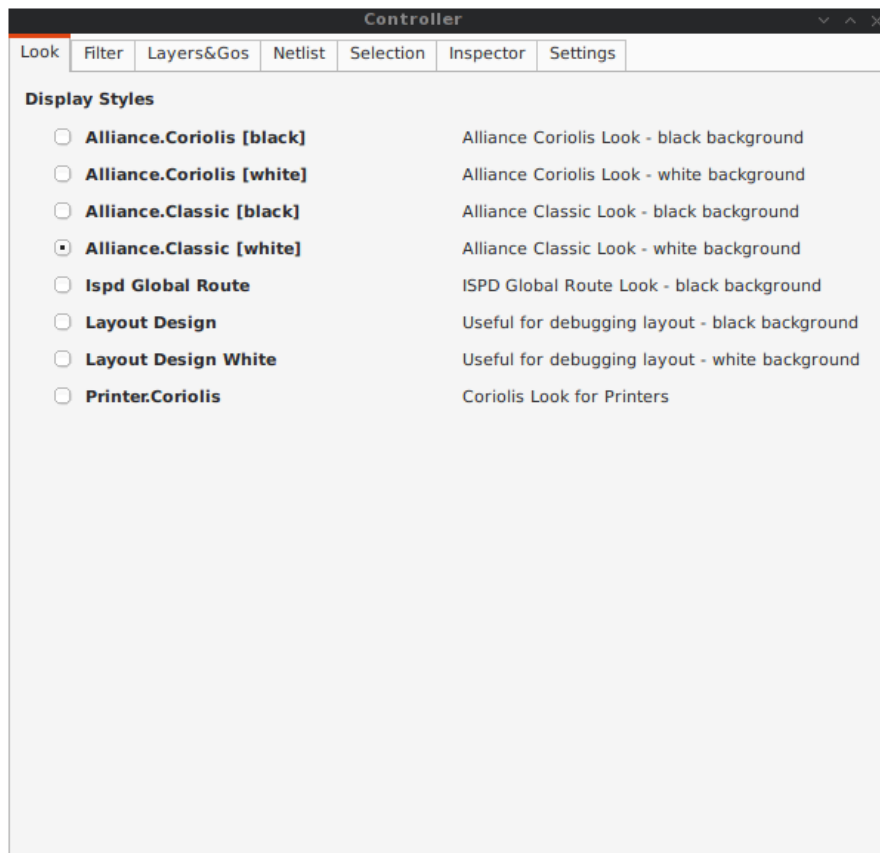
The Controller

The *Controller* window is composed of seven tabs:

1. **The Look Tab** to select the display style.
2. **The Filter Tab** the hierarchical levels to be displayed, the look of rubbers and the dimension units.
3. **The Layers&Go Tab** to selectively hide/display layers.
4. **The Netlist Tab** to browse through the *netlist*. Works in association with the *Selection* tab.
5. **The Selection Tab** allows to view all the currently selected elements.
6. **The Inspector Tab** browses through either the DataBase, the Cell or the current selection.
7. **The Settings Tab** accesses all the tool's configuration settings.

The Look Tab

You can select how the layout will be displayed. There is a special one `Printer.Coriolis` specifically designed for **Printing & Snapshots**. You should select it prior to calling the print or snapshot dialog boxes.



The Filter Tab

The filter tab let you select what hierarchical levels of your design will be displayed. Hierarchy level are numbered top-down: the level 0 corresponds to the top-level cell, the level one to the instances of the top-level Cell and so on.

There are also check boxes to enable/disable the processing of Terminal Cell, Master Cells and Components. The processing of Terminal Cell (hierarchy leaf cells) is disabled by default when you load a hierarchical design and enabled when you load a single Cell.

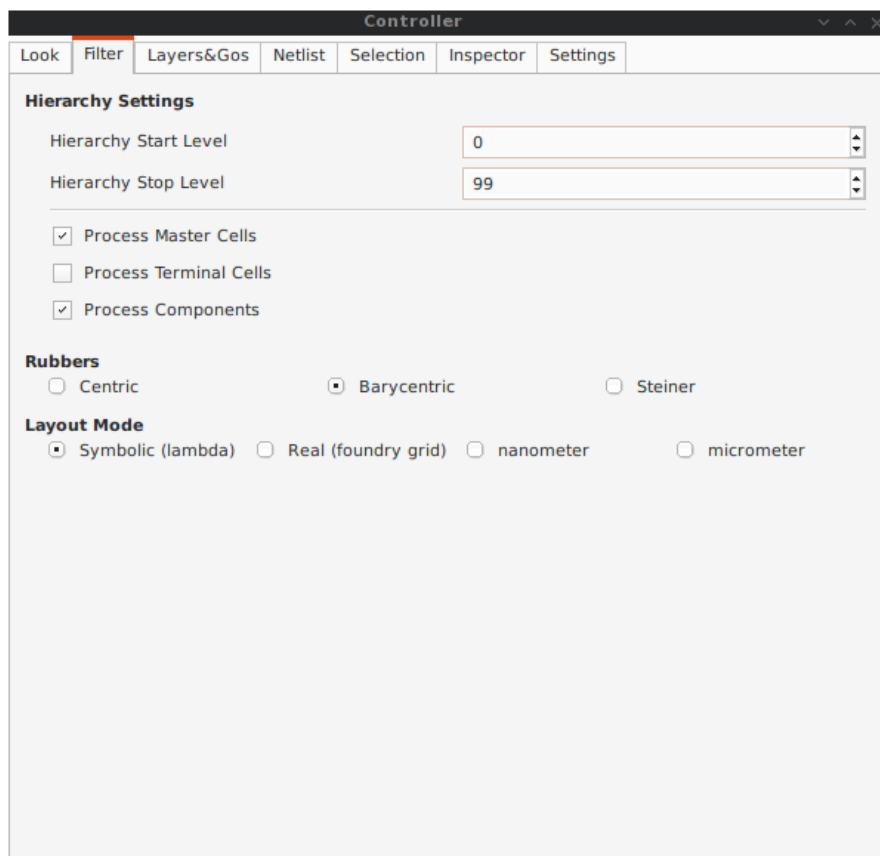
You can choose what kind of form to give to the rubbers and the type of unit used to display coordinates.



Note

What are Rubbers: HURRICANE uses *Rubbers* to materialize physical gaps in net topology. That is, if some wires are missing to connect two or more parts of net, a *rubber* will be drawn between them to signal the gap.

For example, after the detailed routing no *rubber* should remain. They have been made very visible as big violet lines...



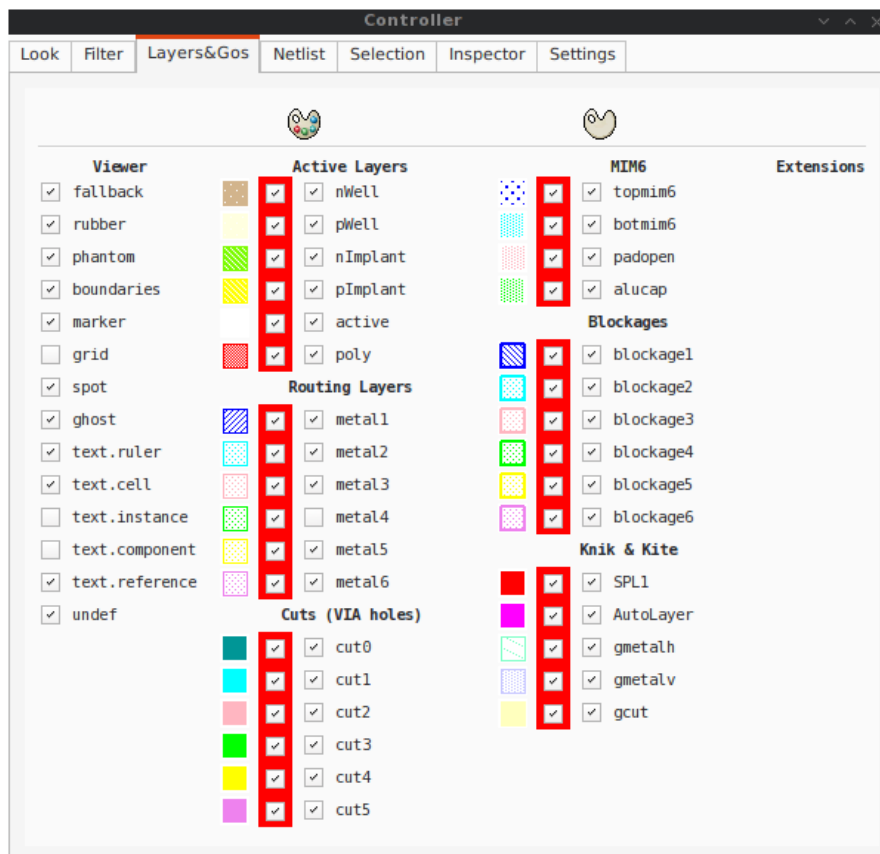
The Layers&Go Tab

Control the individual display of all *layers* and *Gos*.

- *Layers* correspond to true physical layers. From a HURRICANE point of view they are all the *BasicLayers* (could be matched to GDSII).
- *Gos* stands from *Graphical Objects*, they are drawings that have no physical existence but are added by the various tools to display extra information. One good example is the density map of the detailed router, to easily locate congested areas.

For each layer/Go there are two check boxes:

- The normal one triggers the display.
- The red-outlined allows objects of that layer to be selectable or not.



The Netlist Tab

The *Netlist* tab shows the list of nets... By default the tab is not *synced* with the displayed Cell. To see the nets you must check the **Sync Netlist** checkbox. You can narrow the set of displayed nets by using the filter pattern (supports regular expressions).

A very useful feature is to enable the **Sync Selection**, which will automatically select all the components of the selected net(s). You can select multiple nets. In the figure the net `auxsc35` is selected and is highlighted in the *Viewer*.

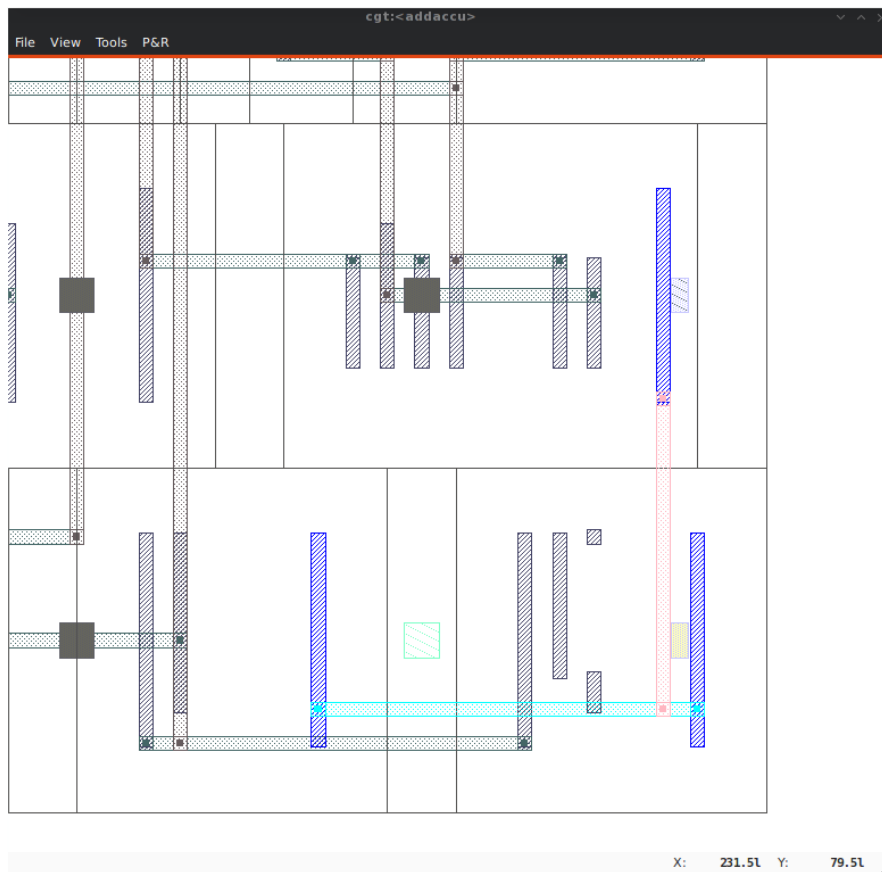
Controller

Look Filter Layers&Gos **Netlist** Selection Inspector Settings

Sync Netlist Sync Selection

Net	Plugs
a(0)	2
a(1)	1
a(2)	1
a(3)	1
auxreg1	2
auxreg2	2
auxreg3	3
auxreg4	4
auxsc1	8
auxsc11	2
auxsc16	3
auxsc18	3
auxsc20	4
auxsc21	4
auxsc22	4
auxsc24	3
auxsc35	3
auxsc36	2
auxsc37	2
auxsc38	2
auxsc39	5
auxsc40	2
auxsc41	4
auxsc43	2
auxsc44	2
auxsc45	2

Filter pattern:

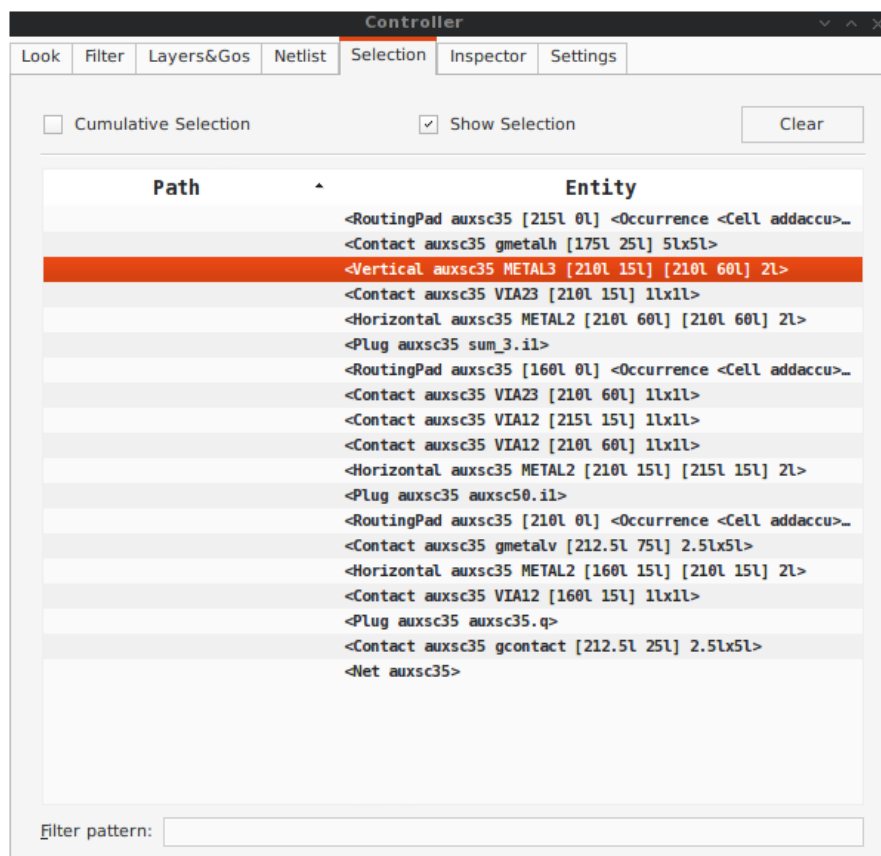


The Selection Tab

The *Selection* tab lists all the components currently selected. They can be filtered thanks to the filter pattern.

Used in conjunction with the *Netlist Sync Selection* you will all see all the components part of *net*.

In this list, you can toggle individually the selection of component by pressing the `t` key. When unselected in this way a component is not removed from the the selection list but instead displayed in red italic. To see where a component is you may make it blink by repeatedly press the `t` key...



The Inspector Tab

This tab is very useful, but mostly for CORIOLIS developpers. It allows to browse through the live DataBase. The *Inspector* provides three entry points:

- **DataBase:** Starts from the whole HURRICANE DataBase.
- **Cell:** Inspects the currently loaded Cell.
- **Selection:** Inspects the object currently highlighted in the *Selection* tab.

Once an entry point has been activated, you may recursively expore all its fields using the right/left arrows.

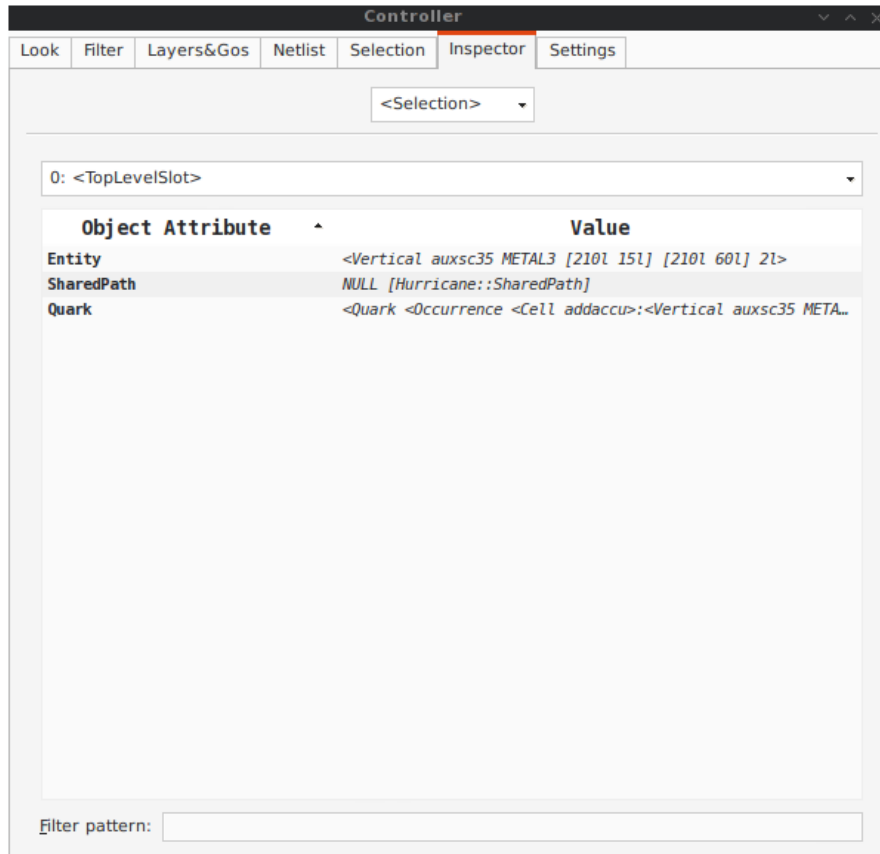


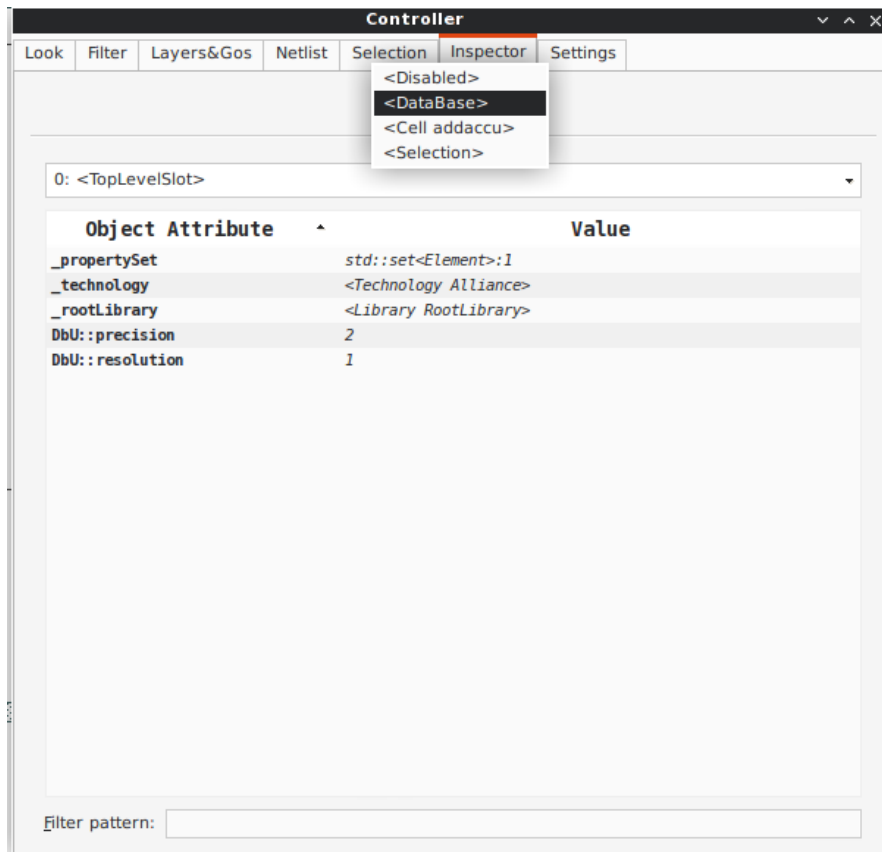
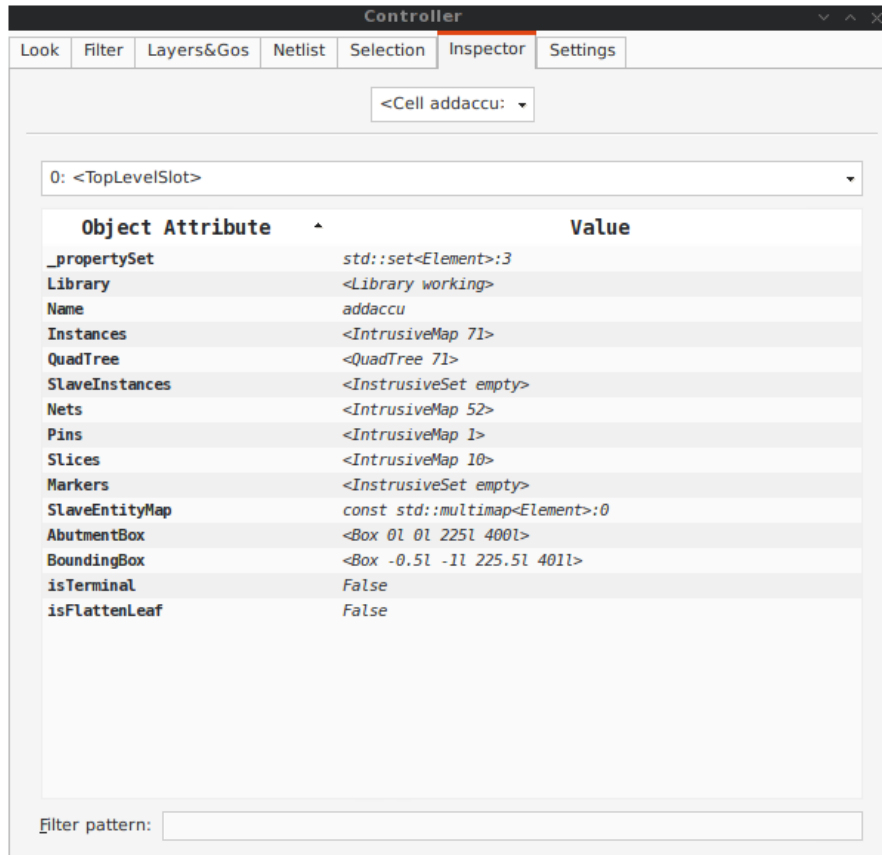
Note

Do not put your fingers in the socket: when inspecting anything, do not modify the DataBase. If any object under inspection is deleted, you will crash the application...

**Note**

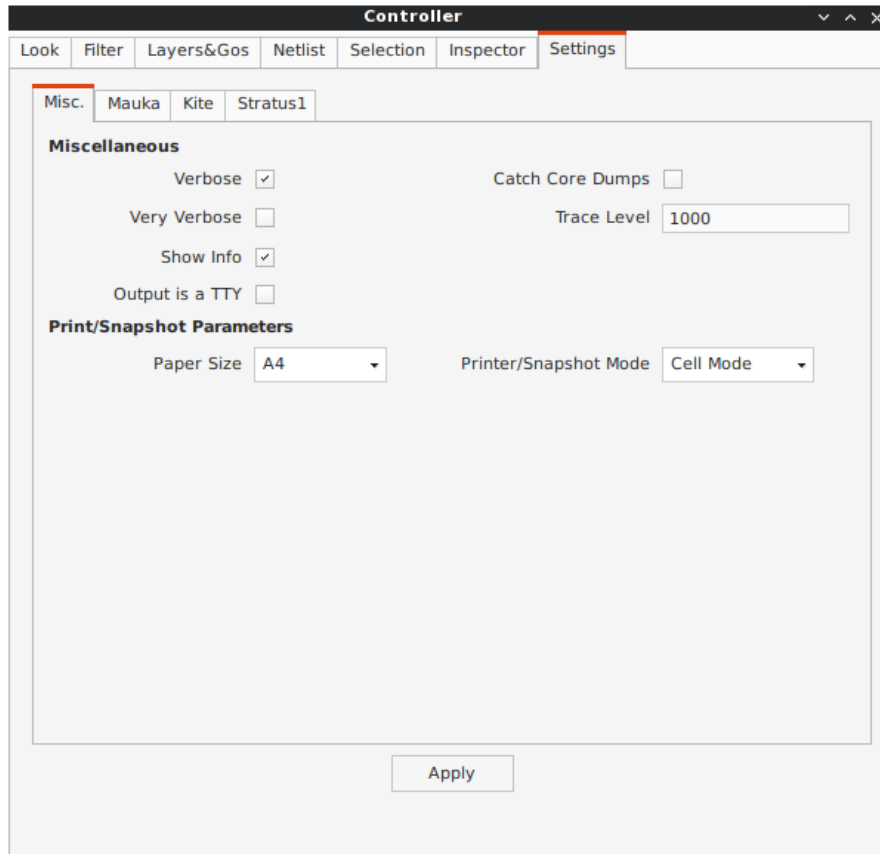
Implementation Detail: the inspector support is done with Slot, Record and getString().





The Settings Tab

Here comes the description of the *Settings* tab.



Python Interface for HURRICANE / CORIOLIS

The (almost) complete interface of HURRICANE is exported as a PYTHON module and some parts of the other components of CORIOLIS (each one in a separate module). The interface has been made to mirror as closely as possible the C++ one, so the C++ doxygen documentation could be used to write code with either languages.

Summary of the C++ Documentation

A script could be run directly in text mode from the command line or through the graphical interface (see [Python Scripts in Cgt](#)).

Aside for this requirement, the python script can contain anything valid in PYTHON, so don't hesitate to use any package or extension.

Small example of Python/Stratus script:

```
import symbolic.cmos
from Hurricane import *
from Stratus import *

def doSomething ():
    # ...
    return

def ScriptMain ( **kw ):
    editor = None
    if kw.has_key('editor') and kw['editor']:
        editor = kw['editor']
        stratus.setEditor( editor )

    doSomething()
    return

if __name__ == "__main__" :
    kw = {}
    success = ScriptMain( **kw )
    shellSuccess = 0
    if not success: shellSuccess = 1

    sys.exit( shellSuccess )
    ScriptMain ()
```

This typical script can be executed in two ways:

1. Run directly as a PYTHON script, thanks to the

```
if __name__ == "__main__" :
```

part (this is standart PYTHON). It is a simple adapter that will call **ScriptMain()**.

In this case, the `import symbolic.cmos` statement at the begining is mandatory.

2. Through **cgt**, either in text or graphical mode. In that case, the **ScriptMain()** is directly called trough a sub-interpreter. The arguments of the script are passed through the `**kw` dictionary.

In this case, the `import symbolic.cmos` statement at the begining may be omitted.

**kw Dictionary	
Parameter Key/Name	Contents type
'cell'	A Hurricane cell on which to work. Depending on the context, it may be <code>None</code> . For example, when run from <code>cgt</code> , the cell currently loaded in the viewer, if any.
'editor'	The viewer from which the script is run, when lauched through <code>cgt</code> .

Plugins

Plugins are PYTHON scripts specially crafted to integrate with `cgt`. Their entry point is a `ScriptMain()` method as described in [Python Interface to Coriolis](#). They can be called by user scripts through this method.

Chip Placement

Automatically performs the placement of a complete chip. This plugin, as well as the other P&R tools expect a specific top-level hierarchy for the design. The top-level hierarchy must contain the instances of all the I/O pads and **exactly one** instance named `corona` of an eponym cell `corona`. The `corona` cell in turn contains the instance of the chip's core model.

The intermediate `corona` hierarchical level has been introduced to handle the possible decoupling between real I/O pads supplied by a foundry and a symbolic core. So the `chip` level contains only real layout and the `corona` and below only symbolic layer.



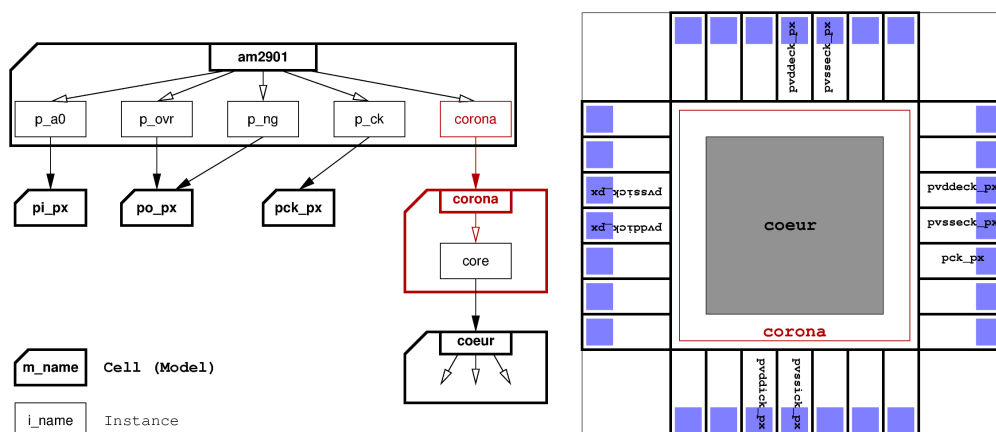
Note

This does not prevent having a design either fully symbolic (pads and core) or fully real.



Note

The `corona` also avoids the router to actually have to manage directly the pads which simplify its configuration and besides avoid to have the pads stuffed with blockages.



The designer must provide a configuration file that defines the rules for the placement of the top-level hierarchy (that is, the pads and the core). This file must be named `ioring.py` and put into the user's configuration directory `./coriolis2/`

Example of chip placement configuration file (for AM2901):

```
from helpers import l, u, n

chip = \
```

```

{ 'pads.ioPadGauge' : 'pxlib'
, 'pads.south'      : [ 'p_a3'      , 'p_a2'      , 'p_a1'      , 'p_r0'
                      , 'p_vddick0', 'p_vssick0', 'p_a0'      , 'p_i6'
                      , 'p_i8'      , 'p_i7'      , 'p_r3'      ]
, 'pads.east'       : [ 'p_zero'   , 'p_i0'     , 'p_i1'     , 'p_i2'
                      , 'p_vddeck0', 'p_vsseck0', 'p_q3'     , 'p_b0'
                      , 'p_b1'     , 'p_b2'     , 'p_b3'     ]
, 'pads.north'      : [ 'p_noe'    , 'p_y3'     , 'p_y2'     , 'p_y1'
                      , 'p_y0'     , 'p_vddeck1', 'p_vsseck1', 'p_np'
                      , 'p_ovr'    , 'p_cout'    , 'p_ng'     ]
, 'pads.west'       : [ 'p_cin'    , 'p_i4'     , 'p_i5'     , 'p_i3'
                      , 'p_ck'     , 'p_d0'     , 'p_d1'     , 'p_d2'
                      , 'p_d3'     , 'p_q0'     , 'p_f3'     ]
, 'core.size'       : ( 1(1500), 1(1500) )
, 'chip.size'       : ( 1(3000), 1(3000) )
, 'chip.clockTree' : True
}

```

The file must contain *one dictionary* named chip.

Chip Dictionary	
Parameter Key/Name	Value/Contents type
'pad.ioPadGauge'	The routing gauge to use for the pad. Must be given as it differs from the one used to route inside the core
'pad.south'	Ordered list (left to right) of pad instance names to put on the south side of the chip
'pad.east'	Ordered list (down to up) of pad instance names to put on the east side of the chip
'pad.north'	Ordered list (left to right) of pad instance names to put on the north side of the chip
'pad.west'	Ordered list (down to up) of pad instance names to put on the west side of the chip
'core.size'	The size of the core (to be used by the placer)
'chip.size'	The size of the whole chip. The sides must be large enough to accomodate all the pads
'chip.clockTree'	Whether to generate a clock tree or not. This calls the Clock-Tree plugin

Configuration parameters, defaults are defined in `etc/coriolis2/<STECHNO>/plugins.conf`.

Parameter Identifier	Type	Default
Chip Plugin Parameters		
chip.block.rails.count	Int	5
	The minimum number of rails around the core block. Must be odd and above 5. One rail for the clock and at least two pairs of power/grounds	
chip.block.rails.hWidth	Int	12 λ
	The horizontal width of the rails	
chip.block.rails.vWidth	Int	12 λ
	The vertical width of the rails	
chip.block.rails.hSpacing	Int	6 λ

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Parameter Identifier	Type	Default
	The spacing, <i>edge to edge</i> of two adjacent horizontal rails	
chip.block.rails.vSpacing	Int	6 λ
	The spacing, <i>edge to edge</i> of two adjacent vertical rails	

**Note**

If no clock tree is generated, then the clock rail is *not* created. So even if the requested number of rails `chip.block.rails.count` is, say 5, only four rails (2^* power, 2^* ground) will be generated.

Clock Tree

Inserts a clock tree into a block. The clock tree uses the H strategy. The clock net is splitted into sub-nets, one for each branch of the tree.

- On **chip** design, the sub-nets are created in the model of the core block (then trans-hierarchically flattened to be shown at chip level).
- On **blocks**, the sub nets are created directly in the top block.
- The sub-nets are named according to a simple geometrical scheme. A common prefix `ck_htree`, then one postfix by level telling on which quarter of plane the sub-clock is located:
 1. `_bl`: bottom left plane quarter.
 2. `_br`: bottom right plane quarter.
 3. `_tl`: top left plane quarter.
 4. `_tr`: top right plane quarter.

We can have `ck_htree_bl`, `ck_htree_bl_bl`, `ck_htree_bl_tl` and so on.

The clock tree plugin works in four steps:

1. Builds the clock tree: creates the top-block abutment box, computes the required levels of H tree and places the clock buffers.
2. Once the clock buffers are placed, calls the placer (ETESIAN) to place the ordinary standard cells, without disturbing clock H-tree buffers.
3. At this point we know the exact positions of all the DFFs, so we can connect them to the nearest H-tree leaf clock signal.
4. Leaf clock signals that are not connected to any DFFs are removed.

Netlist reorganisation:

- Obviously the top block or chip core model netlist is modified to contain all the clock sub-nets. The interface is *not* changed.
- If the top block contains instances of other models *and* those models contain DFFs that get re-connected to the clock sub-nets (from the top level): Changes both the model netlist and interface to propagate the relevant clock sub-nets to the instantiated model. The new model with the added clock signal is renamed with a `_cts` suffix. For example, the sub-block model `ram.vst` will become `ram_cts.vst`.

**Note**

If you are to re-run the clock tree plugin on a netlist, be careful to erase any previously generated `_cts` file (both netlist and layout: `rm *_cts.{ap,vst}`). And restart `cgf` to clear its memory cache.

Configuration parameters, defaults are defined in `etc/coriolis2/<STECHNO>/plugins.conf`.

Parameter Identifier	Type	Default
ClockTree Plugin Parameters		
<code>clockTree.minimumSide</code>	Int	300 λ
	The minimum size below which the clock tree will stop to perform quadri-partitions	
<code>clockTree.buffer</code>	String	buf_x2
	The buffer model to use to drive sub-nets	

Recursive-Save (RSave)

Performs a recursive top down save of all the models from the top cell loaded in `cgf`. Forces a write of any non-terminal model. This plugin is used by the clock tree plugin after the netlist clock sub-nets creation.

A Simple Example: AM2901

To illustrate the capabilities of CORIOLIS tools and PYTHON scripting, a small example, derived from the ALLIANCE **AM2901** is supplied.

This example contains only the synthesized netlists and the `doChip.py` script which perform the whole P&R of the design.

You can generate the chip using one of the following methods:

1. **Command line mode:** directly run the script:

```
dummy@lepka:AM2901> ./doChip -V --cell=amd2901
```

2. **Graphic mode:** launch `cgf`, load chip netlist `amd2901` (the top cell) then run the PYTHON script `doChip.py`.

**Note**

Between two consecutive run, be sure to erase the netlist/layout generated:

```
dummy@lepka:AM2901> rm *_cts*.vst *.ap
```