Coral Dev Board Micro: Mainboard Cover Page

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Engineer: Stefan		Revision: PVT	
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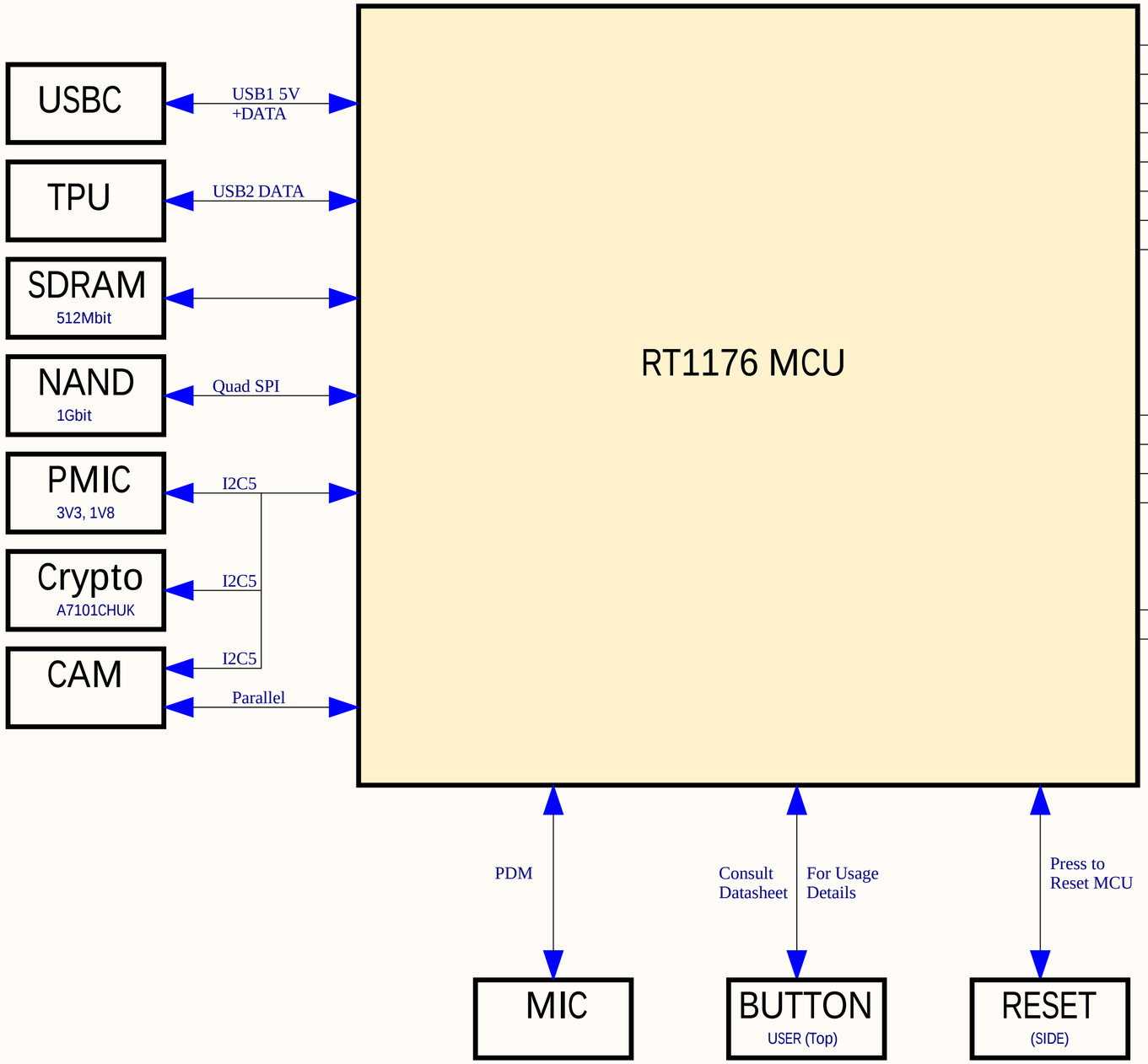
Coral Dev Board Micro: Mainboard Block Diagram

Refer to schematic for pins routed to B2B and default pin MUX



Default Pin Mappings to Header

- ADC (2x)
- PWM (2x)
- DAC (1x)
- I2C (2x)
- SPI (1x)
- UART (1x)
- POWER: 1V8 (2x), 3V3 (1x), VSYS 5V (1x)
- POWER: Coin Cell LP BAK (1x)

Signals used on Add-on boards at Release Time

WIFI

- POWER: 3V3
- WIFI: SDIO (1x) + Control IO
- BT: UART (1x) + Control IO
- DEBUG: JTAG Header Pads

PoE

- POWER: VSYS (I), 3V3 (O)
- ETHERNET: RGMII(IO) + Control IO

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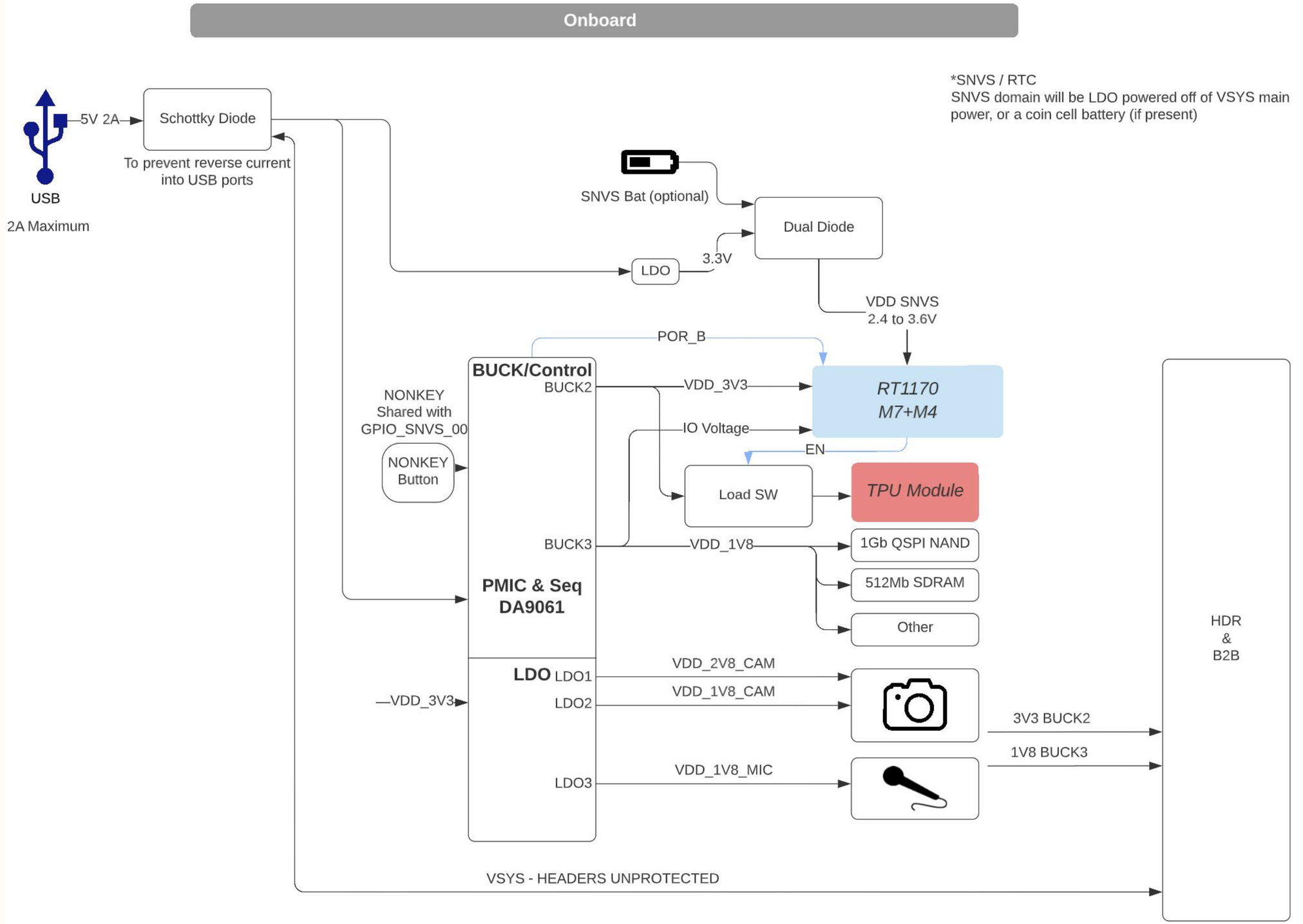
File: 02 BLOCK DIAGRAM.SchDoc		

Coral Dev Board Micro: Mainboard Power Diagram



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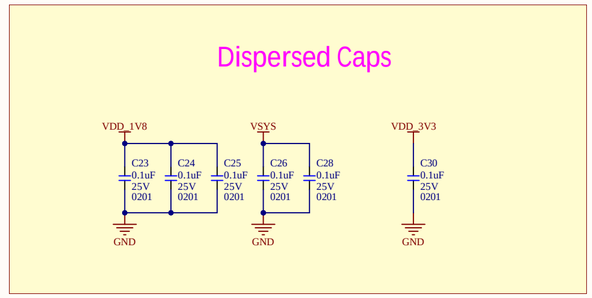
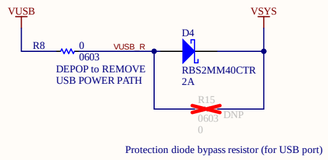
File: 03 POWER DIAGRAM.SchDoc			

Coral Dev Board Micro: Main Power

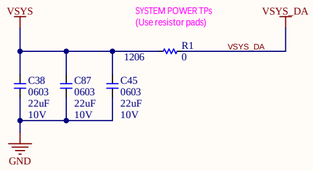
VBAT Power
VSYS Power
VSYS_DA Power

Dispersed Caps

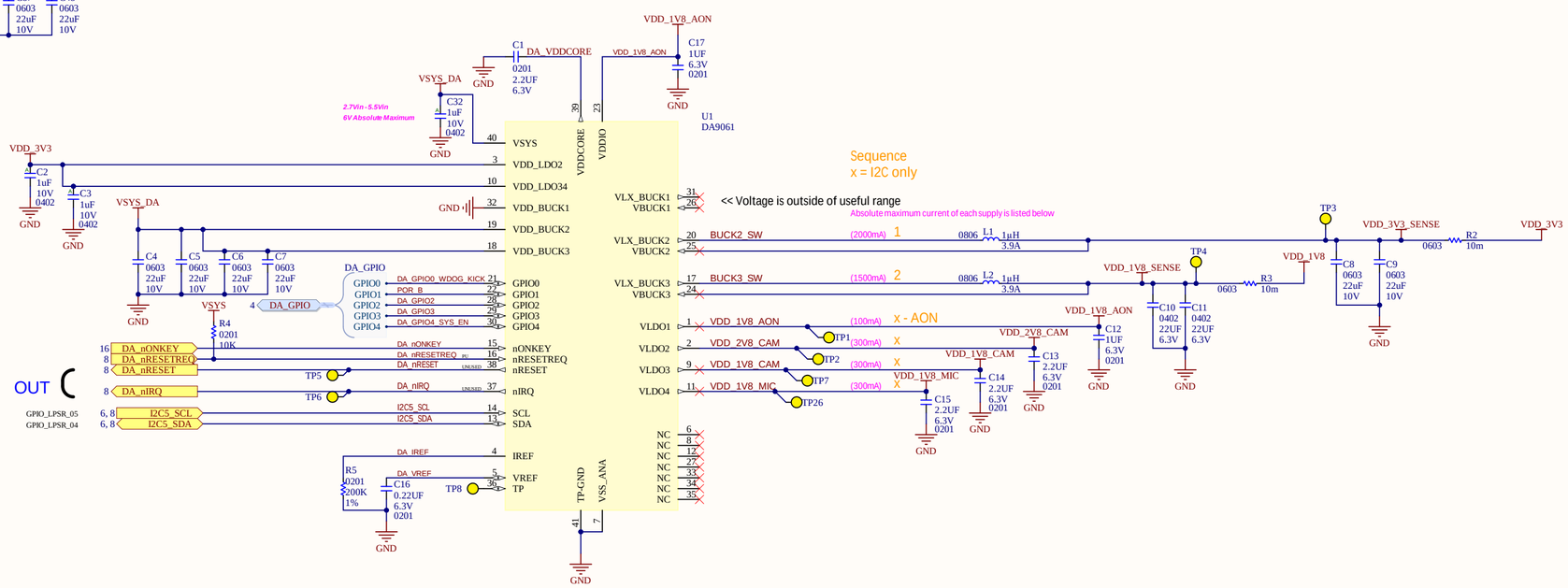




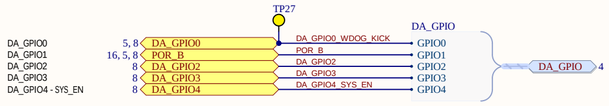
Protection diode bypass resistor (for USB port)



VSYS TO ALL PRIMARY SYSTEM VOLTAGES



WDOG_KICK Optional by customer
DA_GPIO0 can be programmed for watchdog use. Consult the DA9061 Datasheet

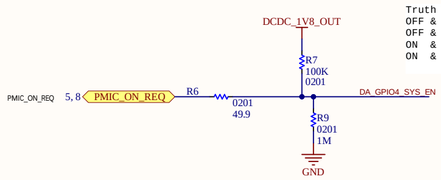


OUT

GPIO_LPSR_05 6, 8 I2C5_SCL
GPIO_LPSR_04 6, 8 I2C5_SDA

Power Control Via Enable (PMIC)

Any TRANSITION on SYS_EN (GPIO4) up or down will cause the DA9061 to smoothly sequence the rails up or down to enter the associated state if it's not already there




```
Truth Table
OFF & RISE | Sequence UP
OFF & FALL | NOTHING (Stays OFF)
ON  & RISE | NOTHING (Stays ON )
ON  & FALL | Sequence DOWN
```

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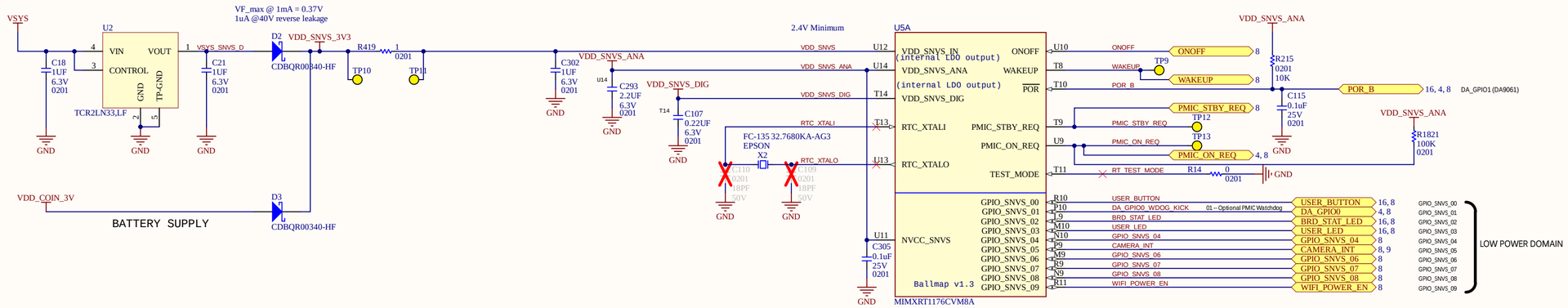
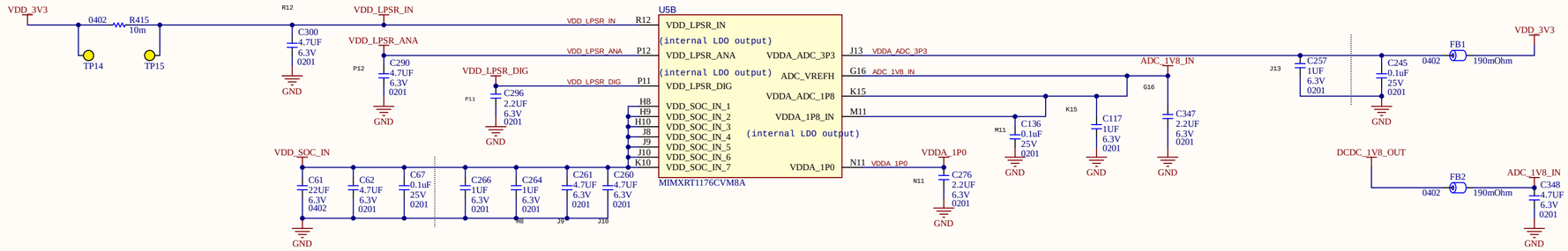
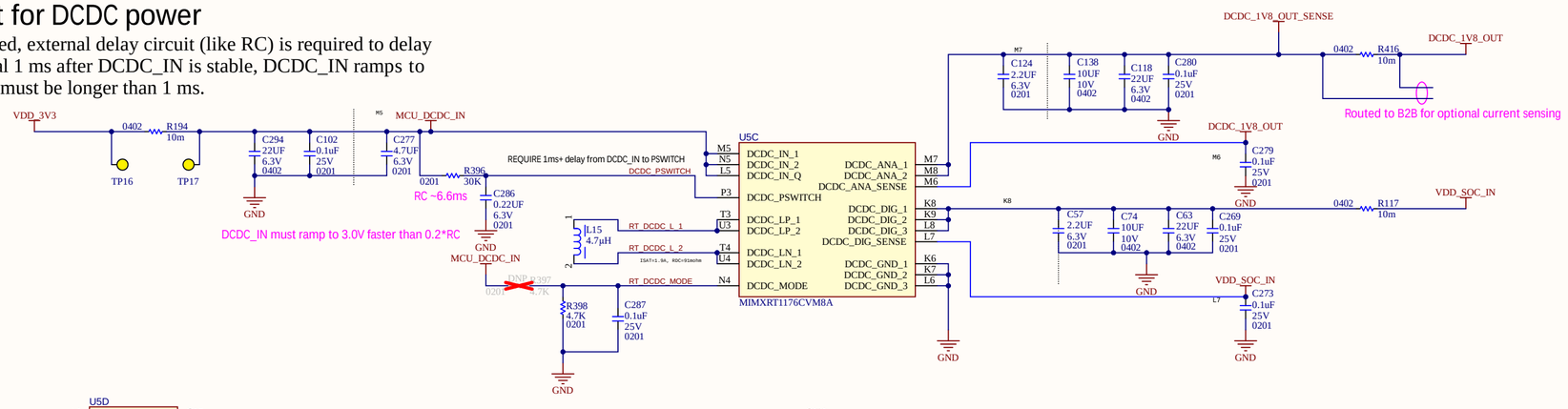
Coral Dev Board Micro: RT1176 PART1

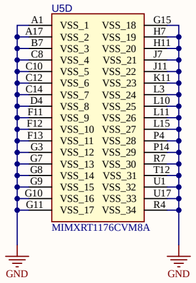


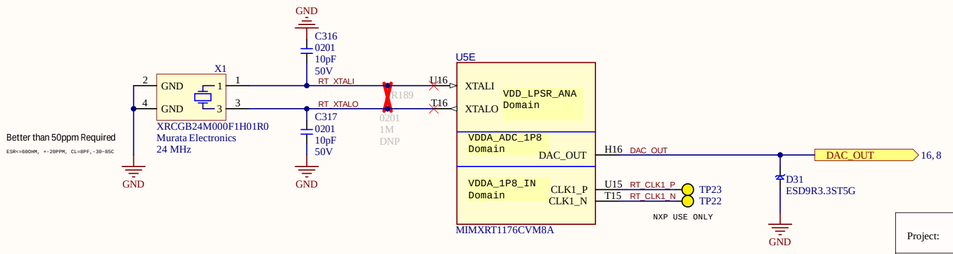


RT1170 HDG Excerpt for DCDC power

When internal DCDC is enabled, external delay circuit (like RC) is required to delay the “DCDC_PSWITCH” signal 1 ms after DCDC_IN is stable, DCDC_IN ramps to 3.0 V within 0.2*RC, and RC must be longer than 1 ms.







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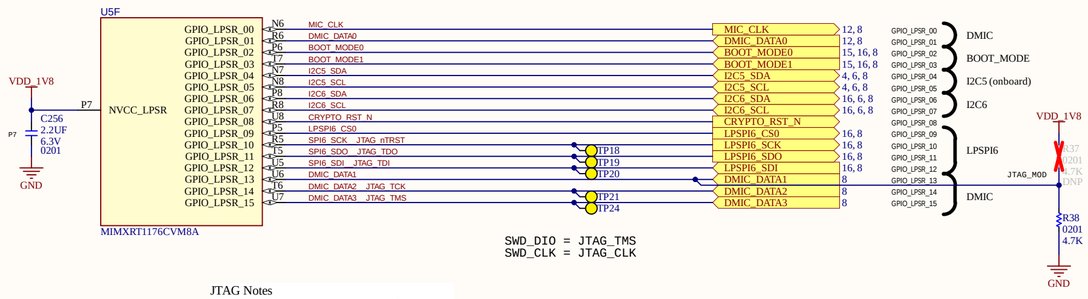
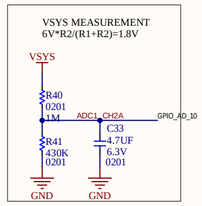
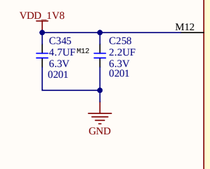
Coral Dev Board Micro: RT1176 PART2

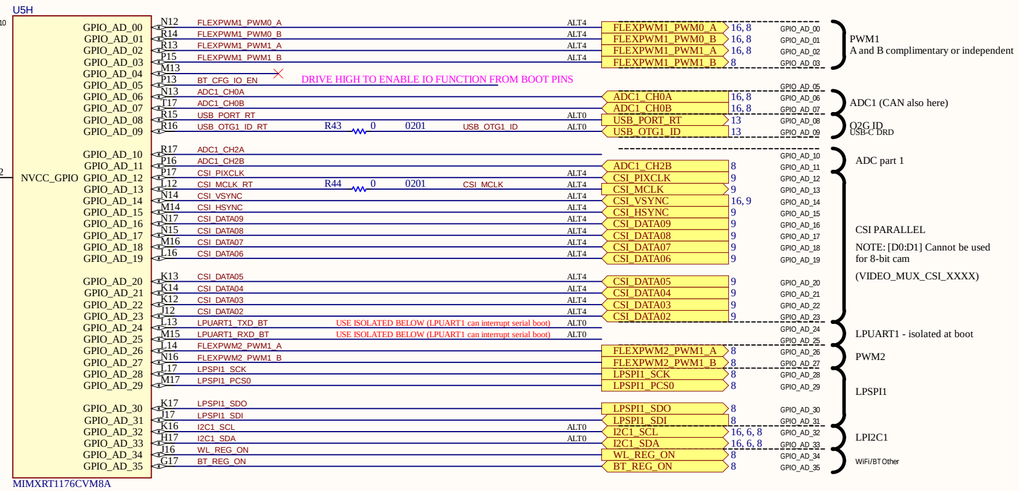


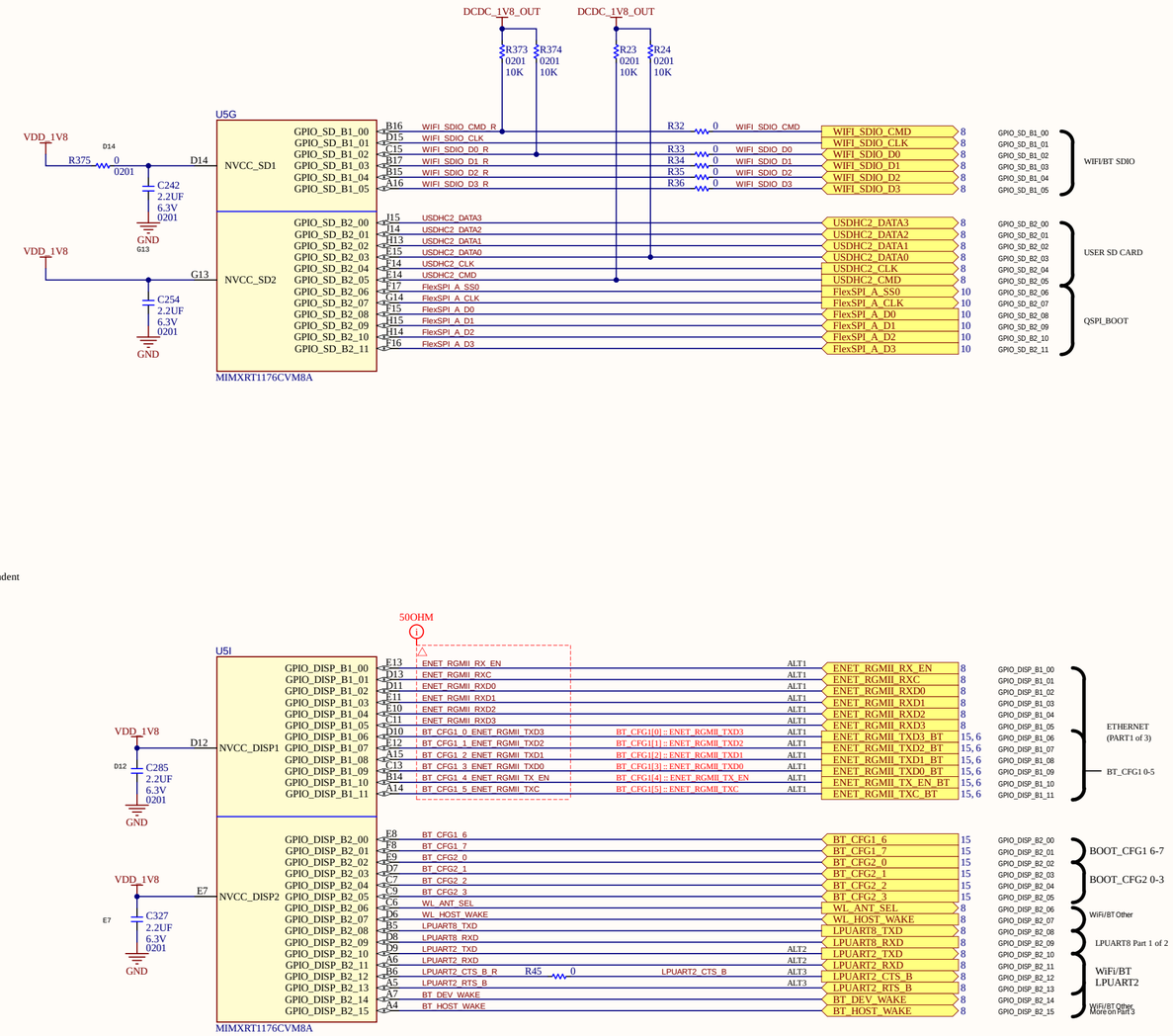
JTAG Notes
-JTAG_TDO internally controlled - Do not pull
-JTAG_TCK :: On chip 20-50k PD
-JTAG_TMS :: On chip 20-50k PU
-JTAG_TDI :: On chip 20-50k PU
-JTAG_TRSTB :: On chip 20-50k PU
-JTAG_MOD :: On chip 20-50k PD

JTAG_MOD
High= IEEE 1149.1 standard
Low= Standard Debug Mode

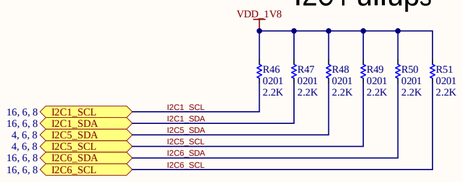




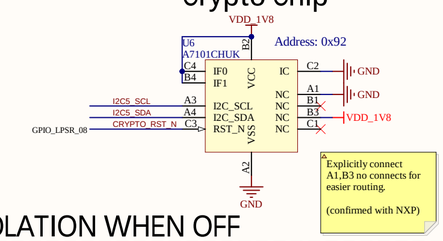




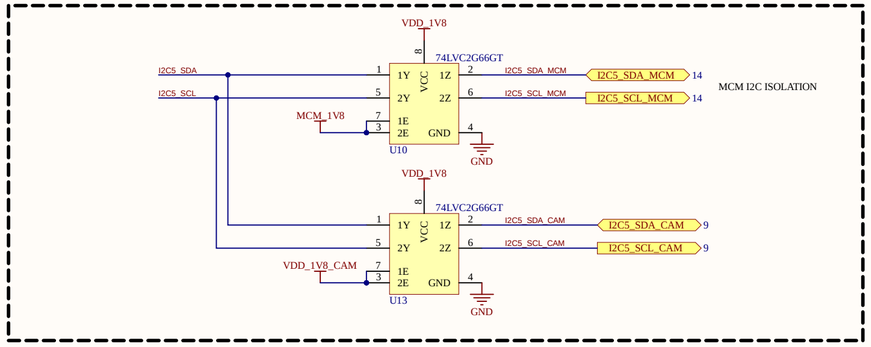
I2C Pullups



Crypto Chip

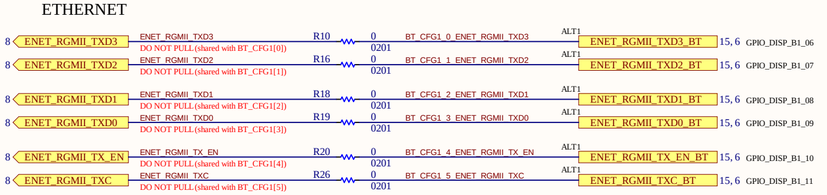


MCM/CAM I2C ISOLATION WHEN OFF

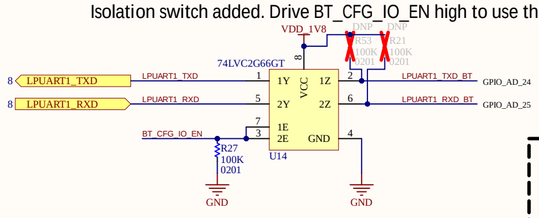


BOOT SIGNAL ISOLATION

ETHERNET



UART cannot be driven at boot time or USB boot mode will never be reached
Isolation switch added. Drive BT_CFG_IO_EN high to use these pins.



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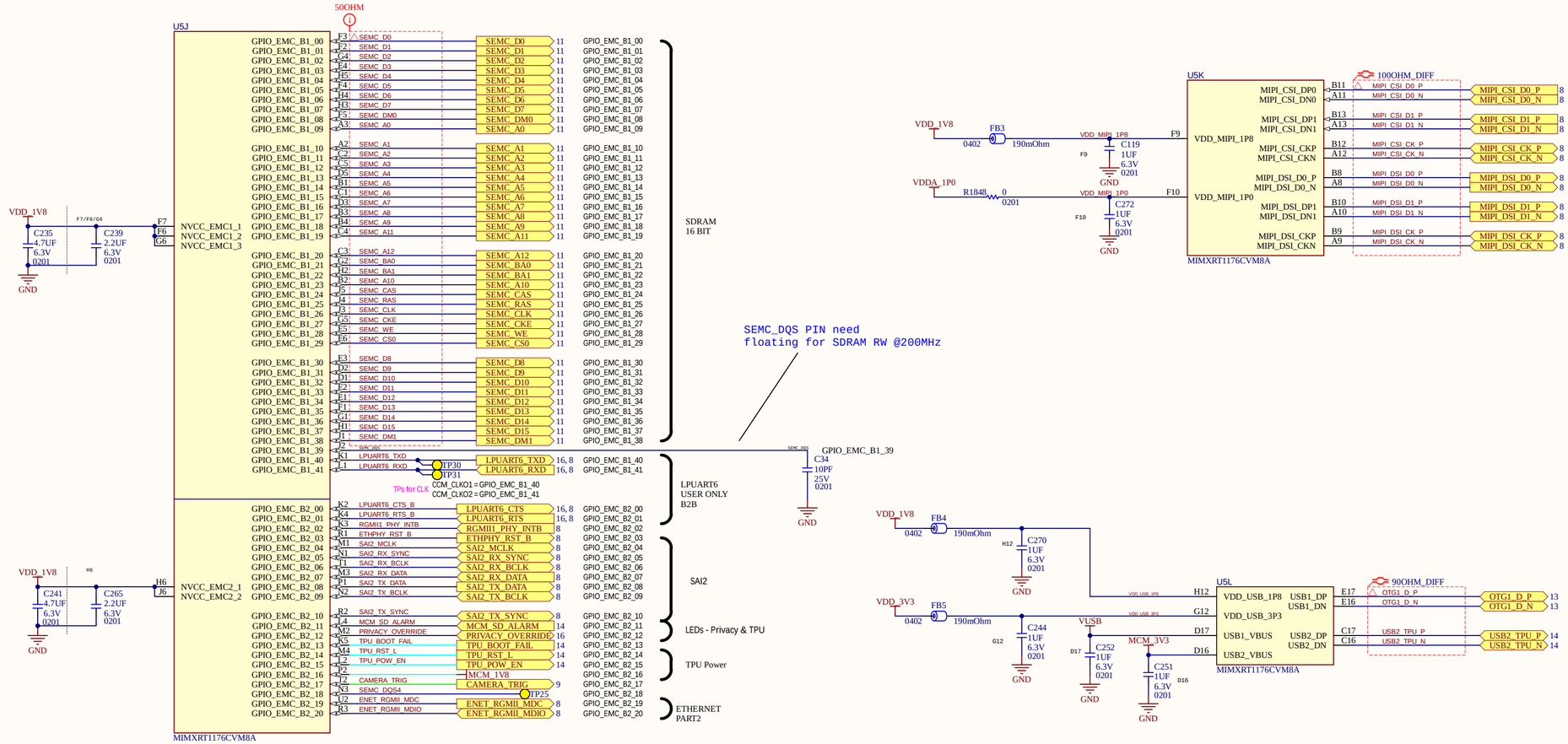
Coral Dev Board Micro: RT1176 PART3



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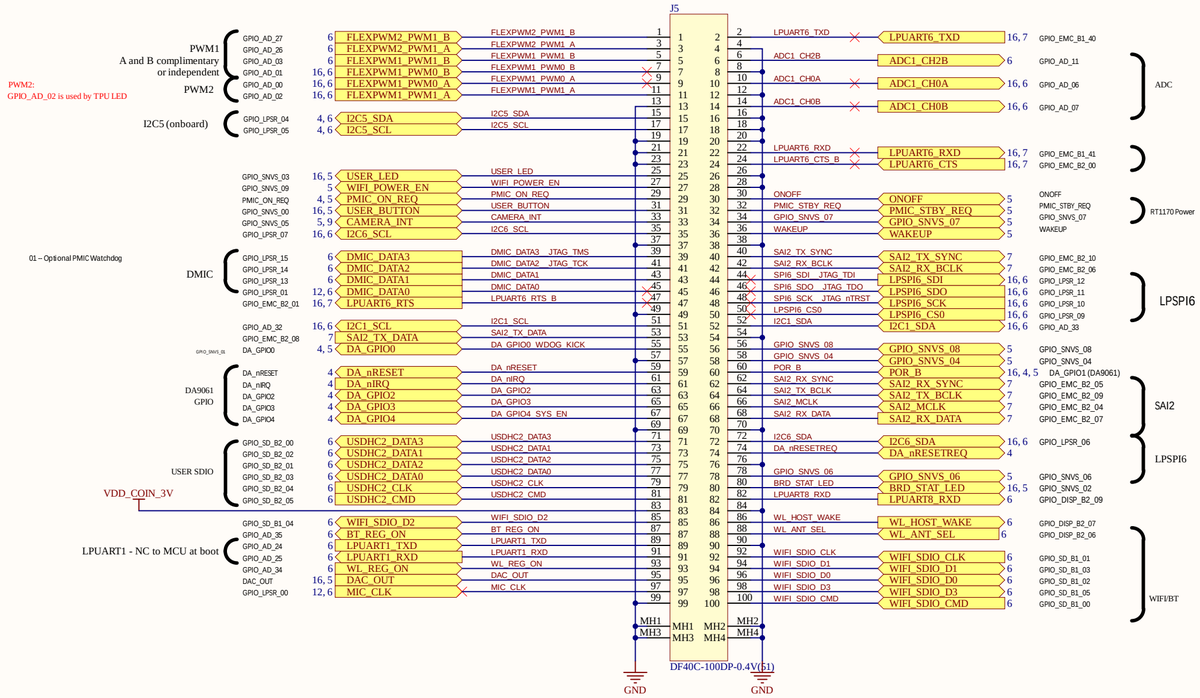
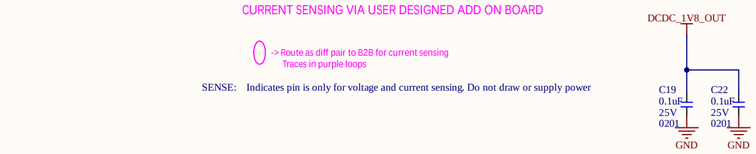
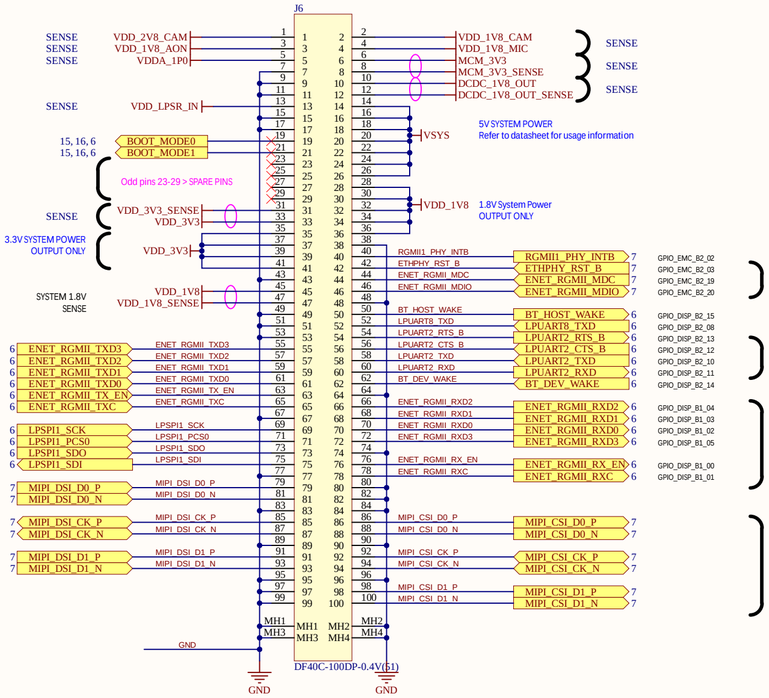
Coral Dev Board Micro: Board to Board Connector

B2B Pinout







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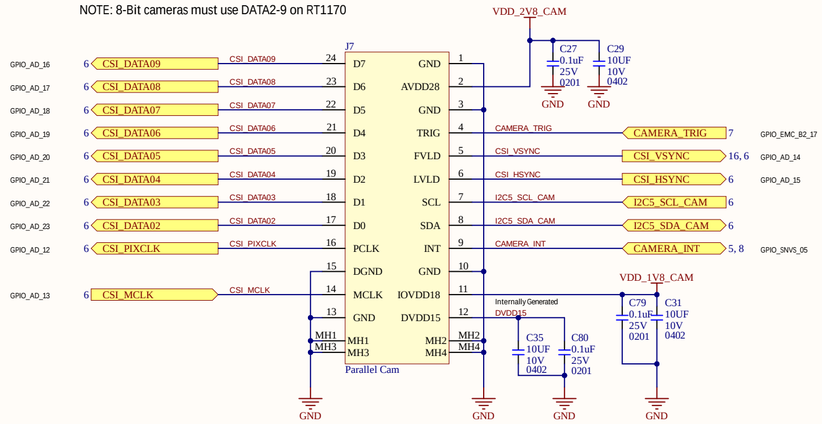
Coral Dev Board Micro: Camera Module

Camera Module Connector



Connector Part Numbers

Molex 5055502420 (receptacle on board)	30 cycles rated
Molex 5055512420 (plug on camera)	30 cycles rated

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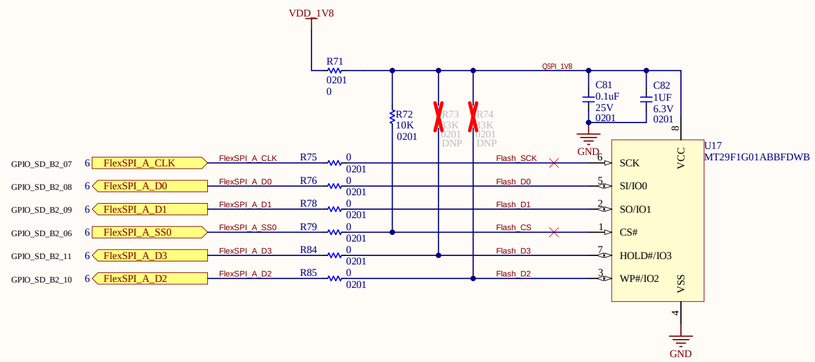
Coral Dev Board Micro: Flash Boot

1V8 QSPI Flash



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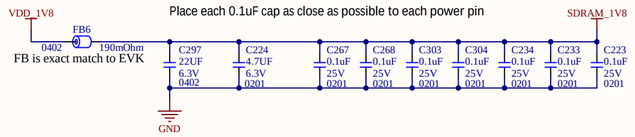
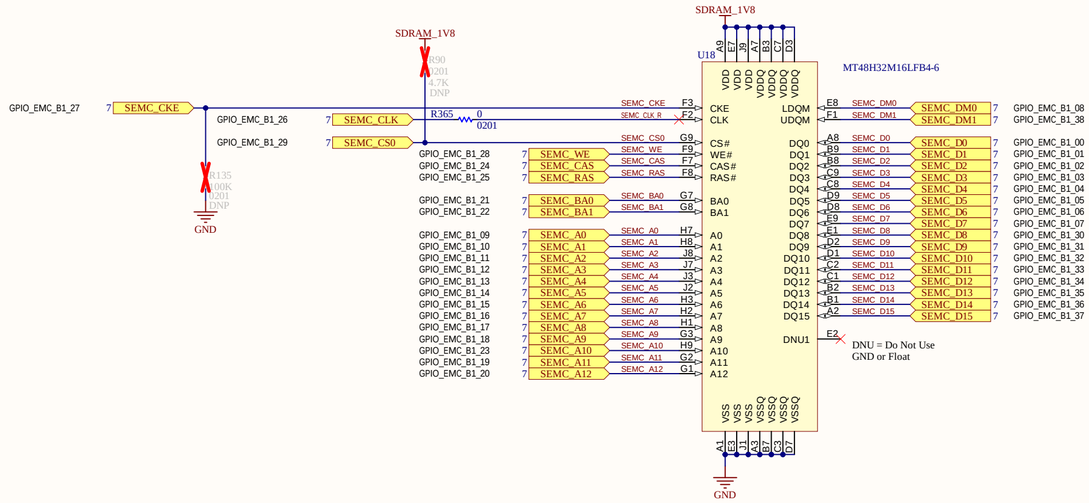
Coral Dev Board Micro: SDRAM



SDRAM (166MHz)



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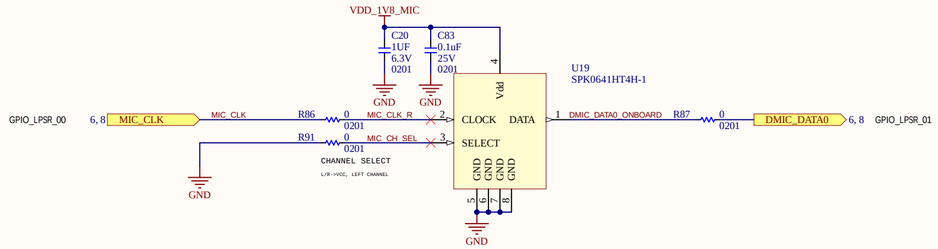
Coral Dev Board Micro: DMIC

DMIC Interface



PDM Channel Info for Microphone

SELECT = GND
-Asserts data on falling edge (MCU samples on CLOCK rising edge)
-By default this is left channel when two mics present on a single data line but can be swapped in the MCU

SELECT = VDD
-Asserts data on the rising edge (MCU samples on CLOCK falling edge)
-By default this is left channel when two mics present on a single data line but can be swapped in the MCU

DMIC 2, 3, 4 SIGNALS sent to B2B

DMIC 1 also sent to B2B. Depop R87 at minimum to use offboard MIC1 left channel.

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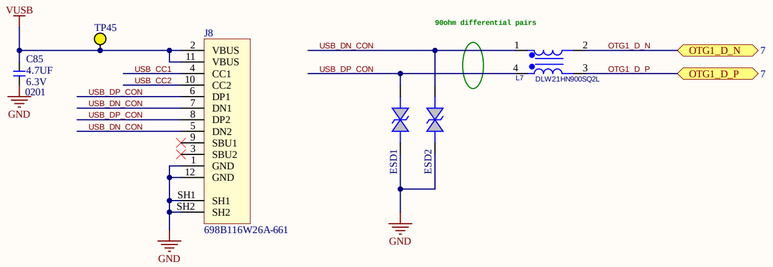
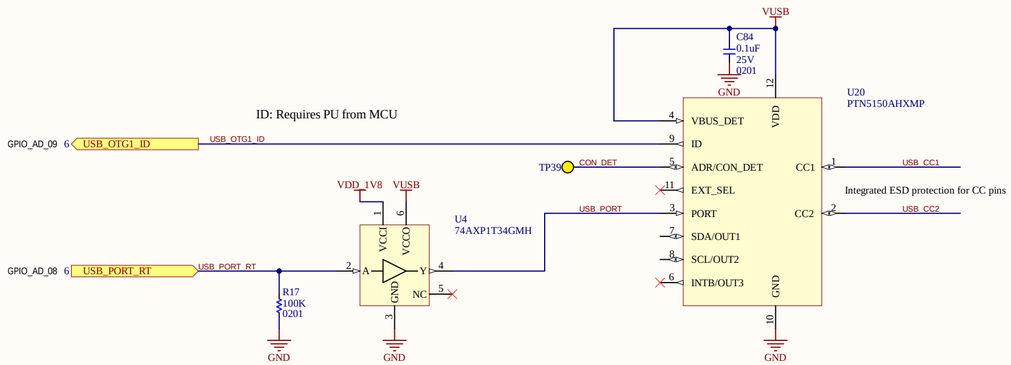
Coral Dev Board Micro: USB

USB-C 2.0 Connector



USB CC Controller



PORT (PTN5150A)
-LOW is UFP
-HIGH is DFP
*DEFAULT: PD for UFP operation

DFP mode is not implemented

```
Host --> ID = GND
Device --> ID = Floating
```

Additional Clarification
- UFP: Upward facing port for USBC. This is sumilar to DEVICE for USB OTG
- DFP: Downward facing port for USBC. Similar to HOST for USB OTG

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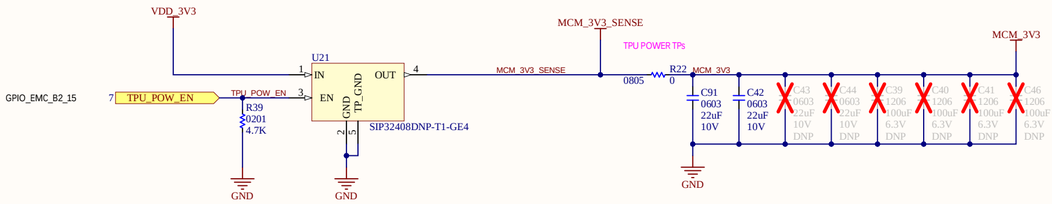
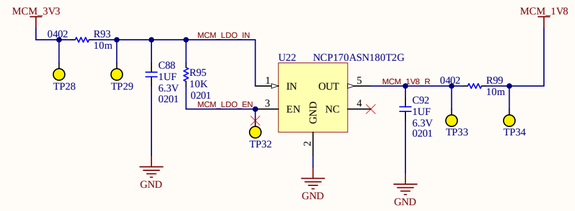
Coral Dev Board Micro: TPU

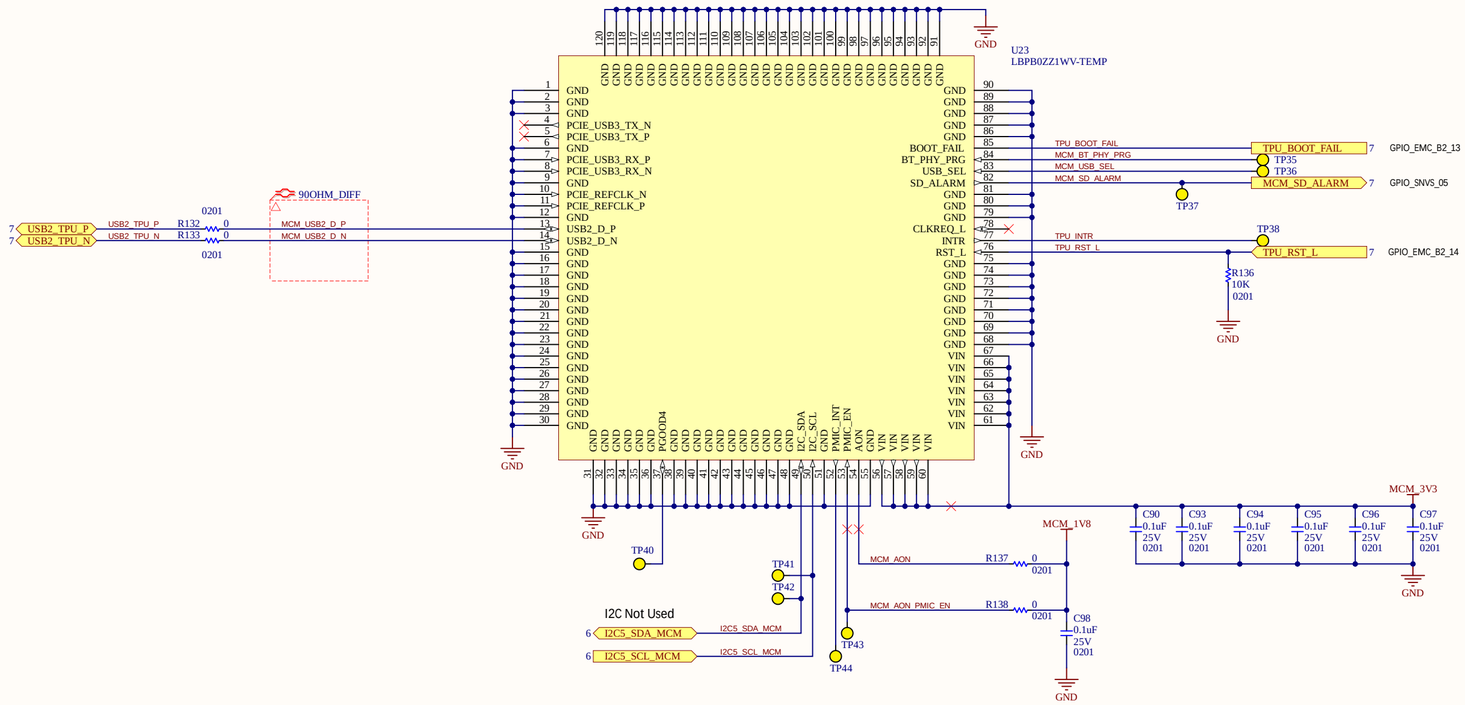
TPU Power Enable Load Switch



TPU 1V8 LDO



Accelerator Module Edge TPU



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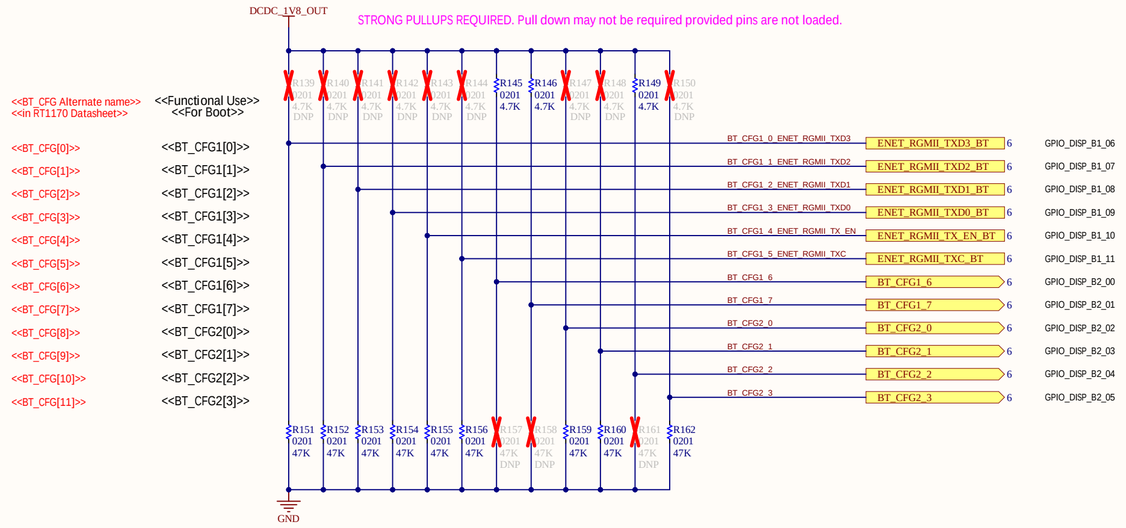
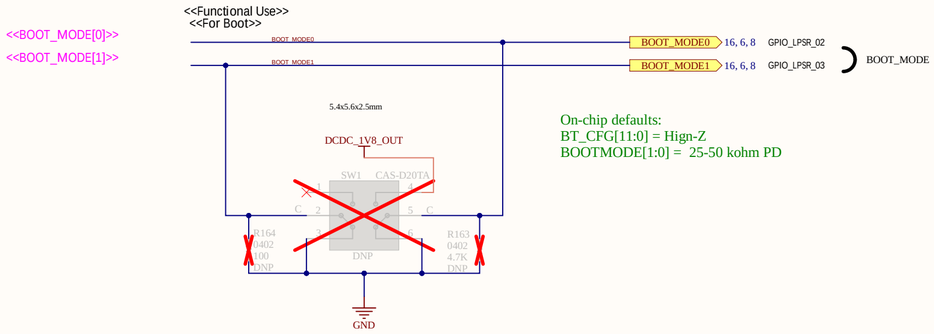
Coral Dev Board Micro: Boot

Boot Configuration

TYPE	BOOT_CFG[11] BT_CFG2[3]	BOOT_CFG[10] BT_CFG2[2]	BOOT_CFG[9] BT_CFG2[1]	BOOT_CFG[8] BT_CFG2[0]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
FlexSPI1 - QSPI NAND	*FLEXSPI_INSTANCE* *0 - FLEXSPI1* *1 - FLEXSPI2*	*CS de-asserted interval between two commands* *0 – 100ns* *1 – 200ns* *2 – 400ns* *3 – 50ns*		*Boot Search Count of FCB and DBBT* *0 - 1* *1 - 2*	*Primary boot device selection* *00 – Serial NOR* *11 – Serial NAND*		*Default safe communication frequency* *0 – High Speed (50MHz)* *1 – Low Speed (30MHz)*	*Column address width* *0 - 12 bits* *1 - 13 bits*	*Hold Time before access to Serial NAND* *0 - Hold time determined by Read Status command* *1 - 500us* *2 - 1ms* *3 - 3ms*		*BOOT_CFG1[1:0]* *0 - 64* *1 - 128* *2 - 256* *3 - 32*	
DEFAULT CONFIGURATION>	RESISTORS : 0 :: FlexSPI1	RESISTORS : 10 :: 400ns		RESISTORS : 0 FCB/DBBT =1	RESISTORS : 11 :: Serial NAND		RESISTORS : 0	RESISTORS : 0 :: 12bit	RESISTORS : 00 :: Hold time by Read Status command		RESISTORS : 00 :: (64)	



External Boot Switch



On-chip defaults:
BT_CFG[11:0] = Hign-Z
BOOTMODE[1:0] = 25-50 kohm PD

Boot MODE pin settings

BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

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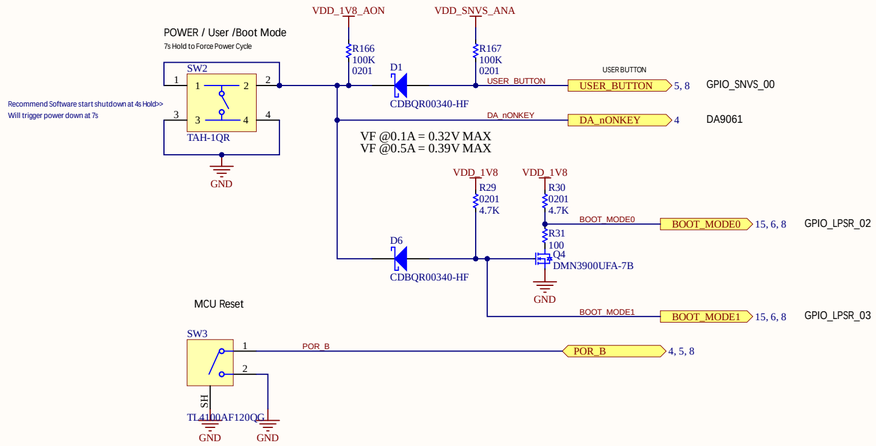
Coral Dev Board Micro: Interface

Buttons

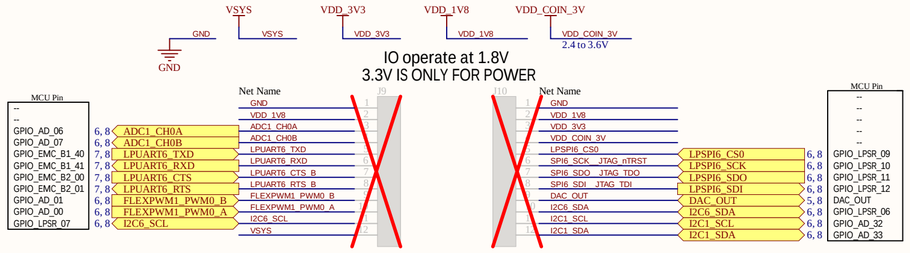


Button usage for entering serial downloader mode

Result is boot mode after soft or hard reset for given button press state

BUTTON	BOOT_MODE1	BOOT_MODE0	Result
OPEN	1	0	*Internal Boot*
PRESSED	0	1	*Serial Downloader Mode*

Header Pinout



Header Pinout Information

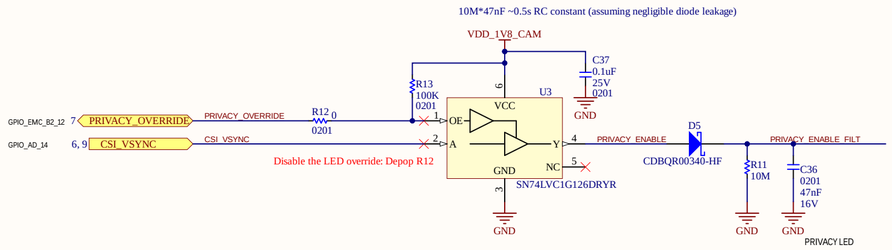
Only one possible pin configuration/ muxing solution is shown for the IMXRT1170 in schematic.

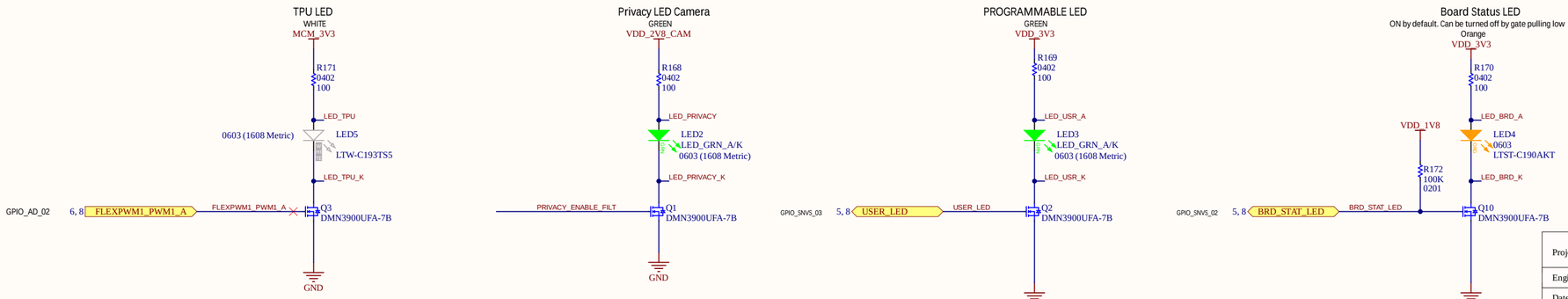
Should the user chooseto MUX pins differently, net names and function may not match schematic.

PRIVACY LED
Power Save Circuit

Use CSI VSYNC to trigger privacy LED.

Discharge RC time constant approximately 500ms. Likely to be shorter due to





Project:	*Coral Dev Board Micro*		
Engineer:	Stefan	Revision:	PVT
Date:	8/12/2022	Sheet	16 of 17
File:	16 INTERFACE.SchDoc		

Google LLC
1600 Amphitheatre Parkway
Mountain View, CA 94043

Coral

Coral Dev Board Micro: Revision History

Revision History

Rev. Code	Date	By	Description
1.0	2022-08-12	Stefan	Schematics prepared for release

Revision History

Rev. Code	Date	By	Description

Project:	Coral Dev Board Micro	*Proprietary and Confidential*	
Engineer: Stefan	Revision: PVT		
Date: 8/12/2022	Sheet 17 of 17		
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